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High Speed Low power RNS DA based FIR filter

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ABSTRACT

The Residue number system (RNS) is known for its parallel arithmetic operation and has been used in recent decades in various important applications, such as digital signal processing. In this paper, we are implementing Distributed arithmetic-based FIR filter using RNS. By using RNS, we increase the speed of the design and at the same time it is more useful for the security purpose. The proposed design is implemented in Xilinx and the proposed design has high speed when compared with the existing architecture.
Keywords: Finite impulse filter, residual number system, distributed arithmetic, multiplier

I. INTRODUCTION

In DSP systems, digital FIR filtering is an omnipotent operation Parhi [1-3]. Since the previous few decades, the multiplication operations that cause increased area, latency, and power have been the key cause of the FIR filter problems. To address this, several techniques and filter topologies have been introduced to build FIR filters by Chen [4]. To save area and power, the FIR filter's multiplier blocks have been replaced with multiplier-less structures. For the FIR filter, several multipliers-less architectures have been devised to boost the filter's performance.

They are divided into memory-based designs [5] and conversion-based methods. The input values and subsequent DA coefficients often take the form of two's complements. According to the author of Naga Jyothi Grande [6], the length of input data determines the DA algorithm's computation time.

When the input data's bit length is large, the architecture's performance will effect. As shown in Table.1 highspeed DSP can be achieved with RNS-based filters. The RNS uses a collection of small numbers to represent a larger number. The critical path time is decreased by the arithmetic calculation utilizing these small integers. A non-weighted number system called RNS, in parallel, divides bigger range binary numbers into several smaller ranges.

RNS is a subtraction, addition, and multiplication carry-free system. RNS system will operate at high speed. An alternative that is considered for weighted 2's complement number system is the Residual number system and for the past five decades, this system is considered one of the most challenging as well as useful number systems. Several desirable features of RNS are examined for various applications of rapid computer arithmetic.

Cryptography, as well as processing of the digital signal, are the two applications of residue number systems.

Table.1

$X_8(1)$	$X_8(2)$	$X_8(3)$	$X_8(4)$
1	1	0	0
0	0	1	0
0	1	1	1
0	0	0	0

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II. PROPOSED RNS DA BASED FIR FILTER

The proposed approach comprises the forward converter unit, the MLDA unit, and the reverse converter unit. In the forward converter section, x(k) input is split into a set of residues called 1, 2, 3, and so on that are obtained using modular arithmetic. Moduli values are predetermined and structured as 2^{n-1}, 2^n,2^{n+1}. The modulo set will be in the style of "9,8,7" for n = 4. The moduli operation is used to transform the coefficients of filter and as well as input signals into residue. The coefficient for the residue filter is one of the inputs to the 2:1 MUX, while the other input is either grounded or set to "0." The output value generated by forward converters is delivered as control line to DA unit of the 2:1 MUX and given to adder to get final output. Finally reverse converter receives outputs of the multiplexer.

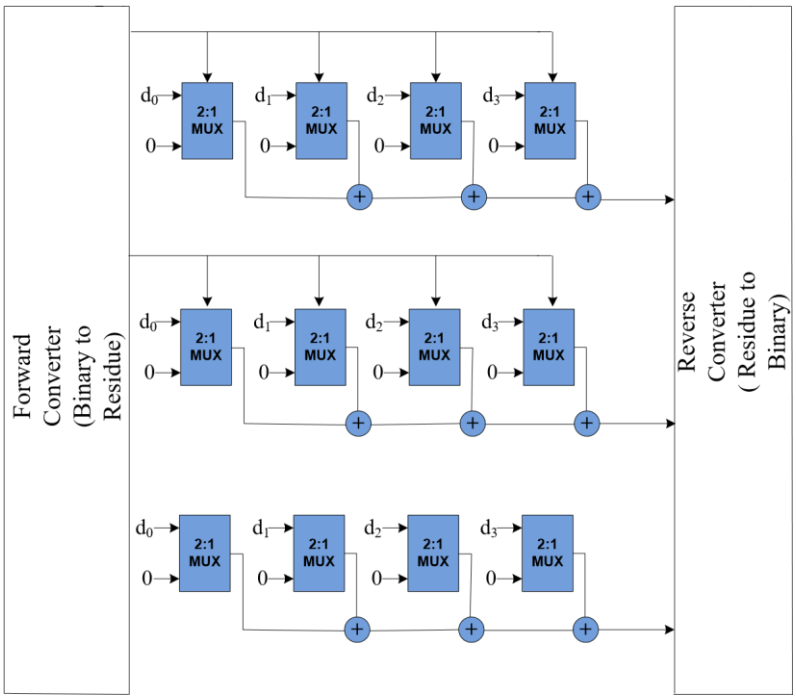


Figure 2 Shows: The Proposed DA based FIR filter

DSP as well as cryptography are some of the uses of RNS (residue number systems). In these applications, mathematical calculations like addition, multiplication, and subtraction play a significant role. Also, with the applications of redundant as well as fault-tolerant facilities, the RNS can identify as well rectify errors. To transmit the information securely without any fault in the communication system, RNS is employed as well as the data sent are in the form of residues. The residues are independent in nature and can reduce errors in the channel from which the information is been transmitted. Therefore, the system's properties of residue number apply to an extensive variety of wireless sensor networks. The Redundant RNS can be employed to identify as well as rectify the fault in a communication system by integrating redundant moduli and conventional moduli sets.

The FIR filter is extensively employed in the applications of DSP and is implemented with the help of a binary number system that encounters high propagation delay. Since n number of addition, as well as multiplications, is carried out, the higher-order FIR filters impose a significant delay. Therefore, DSP minimizes speed [7]. The speed of the FIR filter can be enhanced with the application of RNS. Intra-modulo operation is executed by modulo multiplication. Therefore, there exists no carry propagation between modulo channels. Since it is feasible for a very high dynamic range, an encoding technique that is redundant is designed for eliminating intra carry propagation from mathematical calculations in RNS. The RRNS are used to accomplish a real modulo multiplier in a DSP application.

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III. RESULTS AND DISCUSSION

To substantiate performance measures of the suggested Radio Network System Finite Impulse Response design, experiments are carried out over a variety of moduli sets. The digital design was developed using Verilog HDL, which was then evaluated using ModelSim simulation, vertex-5. Development FPGA board for synthesis, and parameters were created. The result obtained during the synthesis, as well as deviceutilizations, are illustrated in Tables.2 and 3. The test results reveal that speculative Distributed Arithmetic model exploits provide significant path delay reduction with high efficiency of resource efficiency. The predominance of the speculative RNS system that is based on DA in various dynamics of FIR filter topologies was demonstrated by assessing the hardware complexity and utilizing the logical element throughout hardware synthesis.

Table 2 Shows: Comparison of input word length vs performance

Input length size	Moduli set	RNS with speculation and conventional residue computation		RNS with speculation and residue computation	
		Fmax	Area (LEs)	Fmax	Area (LEs)
8 bits	(7,8,9)	57.3MHz	1396	75.48MHz	396
16 bits	(31,32,33)	24.96MHz	1823	29.78MHz	1263

Table 3 Shows: Performance analysis of DA based RNS FIR filter design.

FIR length	conventional residue computation		DA based residue computation	
	Fmax	Area (LEs)	Fmax	Area (LEs)
8 taps	63.46MHz	2096	209.600MHz	2009
16 taps	57.3MHz	57.3	356.125MHz	8193

IV. CONCLUSION

This paper exhibits a comprehensive review of various 2n-1 modulo multipliers with no memory. This research is examined by using the Booth algorithm to improve the performance of 2n-1 modulo multipliers by confining the number of PPs, which is set to 1/3rd for radix-8 Booth-encoded multipliers. Due to hardmultiple occurrences, the 2n-1 modulo multiplier is not often utilized for lower dynamic scales; conversely, it is more effective for power as well as an area for larger dynamic ranges. Due to the presence of hardmultiple, the Booth-encoded multipliers are not often utilized for lower dynamic ranges but it is more effective for power as well as an area for larger dynamic ranges. Other than the modulo multiplier stated above, an encoding has been proposed to prevent intra-carry propagation from arithmetic calculations in RNS because this redundant encoding is best suited for substantially high dynamic range in the field of 2n-1 modulo multipliers.

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