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Low Power VLSI Design of 4-2 Compressors Based on the Compensation Characteristic

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ABSTRACT

Approximate computing is tentatively applied in some digital signal processing applications which have an inherent tolerance for erroneous computing results. The approximate arithmetic blocks are utilized in them to improve the electrical performance of these circuits. Multiplier is one of the fundamental units in computer arithmetic blocks. Moreover, the 4-2 compressors are widely employed in the parallel multipliers to accelerate the compression process of partial products. In this paper, three novel approximate 4-2 compressors are proposed and utilized in 16-bit multipliers. Meanwhile, an error-correcting module (ECM) is presented to promote the error performance of approximate multiplier with the proposed 4-2 compressors. In this paper, the number of the approximate 4-2 compressor's outputs is innovatively reduced to one, which brings further improvements in the energy-efficiency. Compared with the exact 4-2 compressors, the simulation results indicate that the proposed approximate compressors UCAC1, UCAC2, UCAC3 achieve 24.76%, 51.43%, and 66.67% reduction in delay, 71.76%, 83.06%, and 93.28% reduction in power and 54.02%, 79.32%, and 93.10% reduction in area, respectively. And the utilization of these proposed compressors in 16-bit multipliers brings 49.29% reduction of power consumption on average.

Keywords: Error Correcting Module, Compressors, Signal Processing

I.INTRODUCTION

Approximate computing is tentatively applied in some digital signal processing applications which have an inherent tolerance for erroneous computing results. The approximate arithmetic blocks are utilized in them to improve the electrical performance of these circuits. Multiplier is one of the fundamental units in computer arithmetic blocks. Moreover, the 4-2 compressors are widely employed in the parallel multipliers to accelerate the compression process of partial products. In this paper, three novel approximate 4-2 compressors are proposed and utilized in 16-bit multipliers. Meanwhile, an error-correcting module (ECM) is presented to promote the error performance of approximate multiplier with the proposed 4-2
compressors. In this paper, the number of the approximate 4-2 compressor's outputs is innovatively reduced to one, which brings further improvements in the energy efficiency.

Memory systems are protected against transient upsets of data bits using ECCs. Hamming codes are often used in today's memory systems to correct single error and detect double errors in any memory word. In these memory architectures, only errors in the memory words are tolerated and there is no preparation to tolerate errors in the supporting logic (i.e. encoder and corrector).

Driven by the development of applications and the advancement of semiconductor process technology, the complexity, scale, and density of integrated circuits are fast increasing. While it comes with a rapid increase on power consumption, which in turn reduces the lifetime and reliability of devices fortunately, in many applications such as multimedia, digital signal processing, and machine learning the accuracy loss in a proper range does not influence the quality of what we appreciate, due to a limited human perception. This leads to an opportunity that the full precision computing blocks are

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substituted with the approximate counterparts. Since multiplication is a fundamental operation in many digital systems. Various approximate designs are introduced in multipliers. For multipliers of larger bit widths, hybrid-radix Booth encoding method is normally utilized, which focuses on the approximation of the partial products generation While for multipliers of smaller bit widths, as their partial products are usually generated by simple AND gates, the approximation is applied in compression trees, which is arranged to accumulate all the generated partial products. 4-2 compressor is the core of such compression trees, which balances the compression efficiency and hardware cost It gets widely used in fast parallel multipliers to accelerate the compression process. Accordingly, many approximate designs are introduced in 4-2 compressors. In, two novel approximate 4-2 compressors are proposed and embedded into the multipliers. The second design of illustrates the rationality for canceling cin and cout of 4-2 compressors which is also adopted in the subsequent designs. Four designs of dual quality 4-2 compressors are delivered.

II. INTRODUCTION TO TECHNOLOGY

Generally, VLSI technology is used in the devices like computers, cell phones, digital cameras and any electronic gadget. There are certain key issues that serve as active areas of research and are constantly improving as the field continues to mature. VLSI is dominated by the CMOS technology and much like other logic families, this too has its limitations which have been battled and improved upon since years. By taking the example of a processor, the process technology has rapidly shrunk from 180 nm in 1999 to 60nm in 2008 and now it stands at 45nm and attempts are being made to reduce it for 32nm. As the number of transistors increase, the power dissipation is increasing and also the noise. Heat is generated per unit area. New alternatives like Gallium Arsenide technology are becoming an active area of research; future of VLSI seems to change for every little moment.

III. EXISTING SYSTEM

CONVENTIONAL MULTIPLIER AND MULTIPLIERS

In Conventional Multipliers Final Product is obtained by adding partial products along with its previous stage carry outs. With this great amount of delay exists. As number of bits increases Hardware complexity increases, Delay increases and power increases. But in case of Multiplier Large modules can be divided into sub modules and any arithmetic operations can be performed in parallel. Most suitable for Large number of bits where Parallelism, Regularity, Concurrency exists when compare to conventional Multipliers. In conventional multipliers we use AND gates to generate Partial Products, Binary adders for summation of Partial Products and Carry Save Adders for Final Product Summation. But in case of Multiplier to reduce complexity the same 16x16 bit multiplier can be implemented using 8 bit multipliers.

High-speed parallel multipliers are one of the keys in RISCs (Reduced Instruction Set Computers), DSPs (Digital Signal Processors), and graphics accelerators and so on. Array multiplier, Booth Multiplier and Dadda Tree multipliers are some of the standard approaches used in implementation of binary multiplier which are suitable for VLSI implementation. A simple digital multiplier (henceforth referred to as Multiplier in short VM) architecture based on the Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra of Mathematics is presented. An improved technique for low power and high speed multiplier of two binary numbers (16 bit each) is developed. An algorithm is proposed and implemented on 16nm CMOS technology. The designed 16x16 bit multiplier dissipates a power of 0.17 mW. The propagation delay time of the proposed architecture is 27.15ns. These results are many improvements over power dissipations and delays reported in literature for and Booth Multiplier.

IV. PROPOSED SYSTEM

URDHVA TIRYAKBHYAM SUTRA

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The proposed multiplier is based on the "Urdhva Tiryakbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Cross wise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products.

The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers.

This is the general formula applicable to all cases of multiplication. Urdhva Tiryakbhyam means "Vertically and Cross wise", which is the method of multiplication followed.

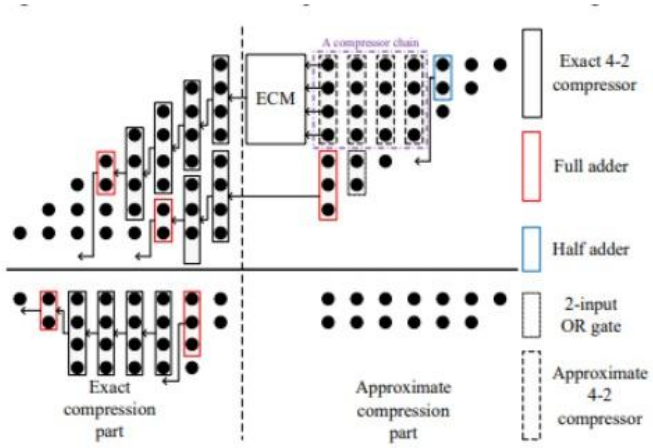


Figure 1: Shows Proposed Dadda Multiplier

Thus, integrating mathematics for the multiplier design will enhance the speed of multiplication operation. The multiplier architecture is based on Urdhva Tiryagbhyam (vertical and cross-wise algorithm) sutra. An illustration of Urdhva Tiryagbhyam sutra Proposed multiplier is designed using the compressed adder blocks which will reduce the power and increases the speed of operation.

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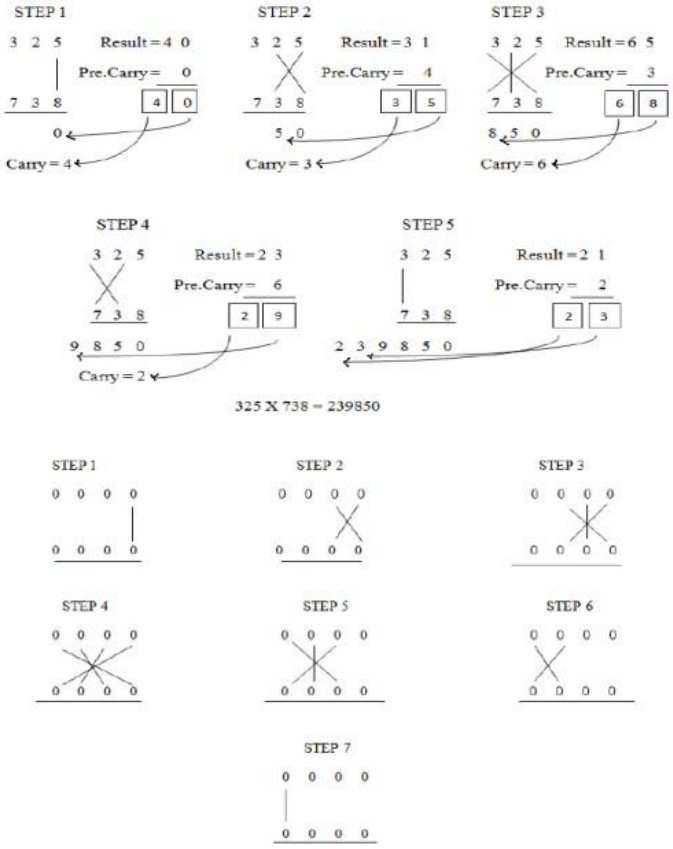


Figure 2: Shows Mathematical Steps

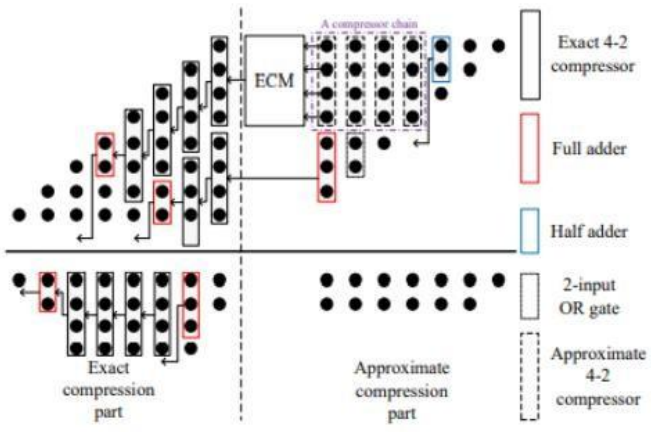


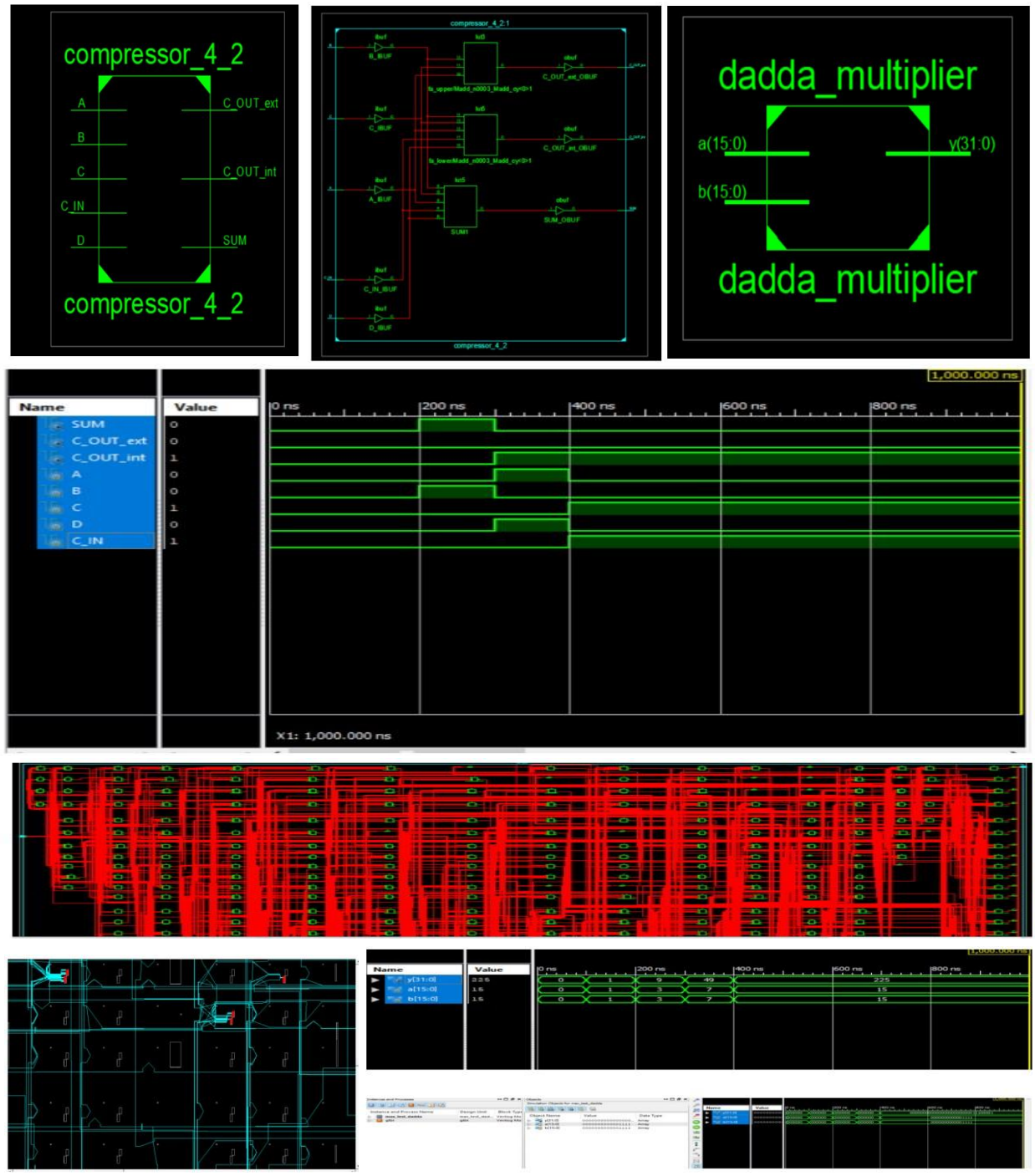
Figure 3: Shows Proposed modified Dadda Multiplier

Thus 16 bit modified Dadda multiplier is constructed and the total number of stages in the second phase is 10. As per the equation the number of row in each of the 10 stages was calculated and the use of half adders was restricted only to the 10th stage. The total number of half adders used in the second phase is 8 and the total number of full adders that was used during the second phase is slightly increased that in the conventional Dadda multiplier Since the 64 bit modified Dadda multiplier is difficult to represent, a typical l0-bit by 10-bit reduction shown in figure 2 for understanding. The modified Dadda tree shows better performance when carry save adder is used in final stage instead

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of ripple carry adder. The carry save adder which is used is considered to be the critical part in the multiplier because it is responsible for the largest amount of computation.

V. RESULTS AND DISCUSSION



Figur4 : Shows Simulation Results and Schematic Diagram

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Compressor based Multiplier has been designed using Reversible logics and the functional correctness of the proposed multiplier. We have proposed a novel high speed architecture for multiplication of two 16 bit numbers, combining the advantages of compressor based reverse logic adders and also the ancient math‟s methodology. A new 4:2 compressor designed with reversible gates architecture was also discussed. Upon comparison of the area occupied by the multiplier and also its speed, with two other popular multipliers. we can conclude that the compressor based reverse math‟s multiplier proves to be a better option over conventional multipliers used in several expeditious and complex VLSI circuits.

In future, both measured and simulation results have shown that systematic design of multiplier with bit size increment of 32 bit and 64 bit with less complexity. If use FPGA for this in future and we will include addition, subtraction and multiplication then it will act as ALU. We can use this in computers. It will decrease power and area.

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