ISSN: 2582 - 6379
Orange Publications
International Journal for Interdisciplinary Sciences and Engineering Applications
IJISEA - An International Peer- Reviewed Journal
2022, December, Volume 3 Issue 4
www.ijisea.org

Two Stage OTA with All Subthreshold MOSFET and Optimum GBW to DC Current Ratio

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ABSTRACT

An approach for the design of two-stage class-AB OTAs with sub-1µA current consumption is proposed and demonstrated. The approach employs MOS transistors operating in subthreshold and allows maximum gain-bandwidth product (GBW) to be achieved for a given DC current budget, by setting optimum distribution of DC currents in the two amplifier stages. Following this strategy, a class AB OTA was designed in a standard 0.5-µm CMOS technology supplied from 1.6-V and experimentally tested. Measured GBW was 307 kHz with 980-nA DC current consumption while driving an output capacitance of 40 pF with an average slew rate of 96 V/ms.
Keywords: DC-DC converter, fuzzy logic controller, electric vehicle

I.INTRODUCTION

The growing interest in wireless sensor networks, biomedical electronics and the Internet of Things continuously demands for novel CMOS circuits and sub systems with limited DC current consumption well below one microampere. Among the CMOS analogue building blocks, the operational transconductance amplifier (OTA) is one of the most popular to its high versatility so that it is frequently instantiated, even several times, within a single integrated circuit, for the implementation of high-accuracy closed-loop configurations. It is consequently of great importance to find suitable OTA architectures and associated design criteria enabling the optimized exploitation of the limited DC current budget, while preserving performance in terms of gain-bandwidth product (GBW) or, alternatively, settling time.

To this aim, subthreshold operation of MOS transistors has been exploited since 1977 until very recently where, for instance, inverter-based subthreshold amplifiers have been proposed. However, inverter-based solutions suffer from inaccurate control of the DC current that therefore depends on process and supply voltage variations. To reduce current and power consumption, alternative architectures and design techniques have also been conceived like body-driven OTAs, dynamic amplifiers or ring amplifiers.

More specifically, a design approach using a class AB two-stage OTA with all transistors in subthreshold region exploiting Miller frequency compensation with pole-zero cancelation (MCPZC) that maximizes the gain-bandwidth. The approach of design an amplifier in a standard 0.5-µm CMOS technology. Measurement results confirm the proposed guidelines, revealing an outstanding performance in terms of small and large-signal characteristics as well as current efficiency.

II. LITERATURE SURVEY

“A 1.1-mW-RX-81.4-dBm sensitivity CMOS transceiver for bluetooth low energy,” J. Masuch and M. Delgado-Restituto,IEEE Trans. Microw.Theory Techn.

This paper presents a fully integrated low-power 130-nm CMOS transceiver tailored to the Bluetooth low energy (BLE) standard. The receiver employs a passive front-end zero-IF architecture, which is directly driven by a quadrature voltage-controlled oscillator (QVCO) without any buffering stage. The QVCO, embedded in a fractional-N phase-locked loop (PLL), employs a passive RC network to cancel the parasitic magnetic coupling between the two cores so as to keep the quadrature phase error below 1.5°.

The PLL exhibits a high loop bandwidth of 1 MHz to sufficiently reduce the frequency pulling effects due to close-by interferers. The transmitter uses a direct-modulation Gaussian frequency-shift keying scheme in which small PMOS-

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based cells modulate the output signal of one of the cores of the QVCO. In the baseband section, the transceiver employs a 4-bit phase domain ADC based on novel linear-combiner topology to generate the required phase rotations.

The proposed combiner operates in current domain and does not employ resistors, leading to a power- and area-efficient demodulator implementation. The complete receiver achieves a sensitivity of - 81.4 dBm and fulfills the BLE requirements on interference blocking.

III. PROPOSED METHOD

In this paper presents a operational trans-conductance amplifier (OTA) to provide a novelty for an ultralow voltage (ULV), ultralow power (ULP). An approach for the design of two-stage class AB OTAs with sub-1µA current consumption is proposed and demonstrated. The approach employs MOS transistors operating in subthreshold and allows maximum gain-bandwidth product (GBW) to be achieved for a given DC current budget, by setting optimum distribution of DC currents in the two amplifier stages. Thus, a straightforward class of AB low power efficient ULV structure have been acquire, which can work on the supply voltages below the threshold of the MOS transistors used. While simultaneously providing the common more range of the input rail to rail. The existing method of OTA based architecture was developed at 500nm CMOS technology using 1.6V. In the proposed method of Two Stage OTA architecture was developed at 45nm using 0.8V and 65nm using 1.2V CMOS technology, finally this work as developed in Tanner EDA tool, and proved the comparison of delay and power consumptions.

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The schematic diagram of the class AB OTA utilized in this brief is depicted in Fig. 1. It is based on a folded-cascode input stage with p-channel source-coupled pair (M0-M10) and a common source class-AB second stage (M11-M12), with Mbat and Cbat providing DC biasing and AC driving for transistor M12, as a result of the so called quasi-floating gate (QFG) approach.

Transistors Mb1-Mb6 implement a conventional bias network. For the low current application target, all transistors are biased in subthreshold regime. Fig. 1 shows the simplified equivalent small-signal circuit of the OTA where gmi, Roi, and Coi are the i-th stage transconductance, output resistance and output apacitance.Specifically, the input-stage transconductance is gm1 = gmM1 = gmM2 and the output transconductance is gm2 = gmM11+ gmM12. 1 CL is the load capacitor that also accounts for Co2. The frequency compensation branch is implemented by the Miller capacitor CC in series with the nulling resistor RC.

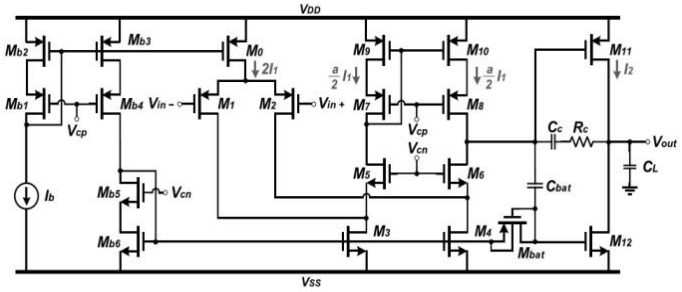


Figure 1: Shows the Proposed Method

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IV. CONCLUSION AND FUTURESCOPE

A methodology to design subthreshold two-stage CMOS OTAs with optimized GBW to DC-current ratio is presented. The optimization process relates the first and second stage bias currents with the compensation capacitors as well as other design constraints such as load capacitance, output first stage capacitance and phase margin. Through this ratio, GBW is maximized for a given current budget, increasing both FOMS and FOML. The proposal has been verified in class-AB OTA implemented with the QFG technique, improving the small and large-signal performance with no additional power increment. In order to verify the whole guidelines, a 0.5-µm test chip prototype has been simulated and fabricated, demonstrating the proposed methodology and exhibiting outstanding results. Low power is becoming the key research area in today's electronics industry. The low power consumption is becoming an important parameter in battery operated devices as speed, area and gain. So we have to design such an efficient circuit which will provide us high Gain, high Unity Gain Bandwidth, high slew rate with the minimum power consumption. We can even try different techniques from the literature to implement with our design to get the better performance.

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