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Design and Implementation of CORDIC Algorithm

A.Hari kiran[1], G.Naga Jyothi[2]
PG Scholar[1], Professor[2]
Department of Electronics and Communication Engineering
Golden Valley Integrated Campus
Angallu, Madanapalli, Andhra Pradesh, India

ABSTRACT

This work introduces a Coordinate Rotation Digital Computer (CORDIC) algorithm for efficient hardware implementation of mathematical functions which can be carried out in a wide variety of ways for many digital signal processing applications. The CORDIC is a single unified algorithm for calculating many elementary functions such as trigonometric, hyperbolic, logarithmic function, exponential functions, multiplication, and division and so on. In this paper, a novel low power, low area, and high throughput fixed-point CORDIC algorithms are proposed. The standard CORDIC is also implemented for comparing the synthesis results. The proposed architecture scaling has been done using low area and low power scale factor correction unit (SFCU). A low ADP SQRT- CSLA based ADD/SUB unit is proposed to overcome the disadvantages of the basic ADD/SUB unit used in the standard CORDIC. The ROM lookup table size is also reduced to half. Extensive simulations are per- formed to verify the functionality. The standard and proposed CORDIC architectures are simulated in cadence NC launch and synthesized in cadence RC tool using TSMC GPDK 45nm technology and area, power and delay are calculated. The area and power consumption of proposed CORDIC architecture are less when compared with standard CORDIC design.

Keywords: CORDIC, adder, parallel, Read only memory, multiplication.

I. INTRODUCTION

Due to various advantages, such as the ability to perform multiple instructions in multiply accumulate in a single cycle and the lack of a need for a significant number of addressing modes, digital signal processing (DSP) plays a more important role than microprocessors. The speed of the microprocessors is very slow when compared to the online DSP applications, but they are more flexible and less expensive. Computer designs are used to boost speed and decrease hardware architectures at cheap costs, making them more competitive, in order to get rid of this recongurable logic for the conventional software strategy. Many algorithms are tuned for microprocessor-based systems and are not effectively suited for hardware platforms. System solutions based on hardware are not better than system solutions based on software.

The more popular and appropriate software system solutions. A class of iterative solutions for mathematical functions and trigonometric functions is one of these hardware and architecturally efficient algorithms. To carry out the operation in these, block of shifts and adders are used. The vector rotation is used to accomplish the trigonometric operations. CORDIC is going to use trigonometry. The second function, which uses the incremental expression of the desired function, is the square root function. An expansion of the hardware design can easily do the square root calculations. The CORDIC function will have an additional bit of accuracy for each iteration. CORDIC was an attractive choice for computing elementary functions instead of using various polynomial methods.

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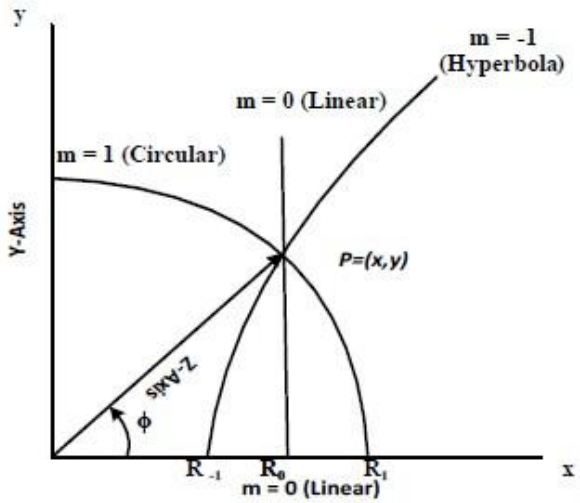


Figure1: Shows CORDIC

CORDIC first appeared in hardware in HP's HP 35 pocket calculator, the Intel 8087 arithmetic coprocessor, RADAR signal processors, and Robotics. The Coordinate Rotation Digital Computer (CORDIC) method was developed by Walther [2] and introduced by Volder [1] for the first time in 1959. Since then, CORDIC has been the subject of more research. Numerous computationally complicated mathematical functions, including:

1. The trigonometric function, are evaluated by the university CORDIC algorithm using coordinate rotations.
2. Hyperbolic operation
3. Exponential behaviour
4. Logarithmic procedures
5. Multiplication
6. Division

II. PROPOSED DESIGN

Due to its special natural property, CORDIC is a powerful algorithm for performing basic operations that take the form of (a b >> 2) and has a straight forward hardware architecture. Hardware multipliers and dividers were relatively expensive at the time the CORDIC was developed. When compared to the conventional approach, the CORDIC algorithm can be implemented with less hardware design and is better suited for high-speed, low-cost applications. The more flexible CORDIC method was primarily employed in digital real-time navigation applications. A step-by-step arrangement of micro-rotations that results in a complete rotation by a known angle as in the rotation operation is, in essence, the fundamental computing technique utilised in both vector and rotation operations. If not, the vectoring process will result in zeroing the vector's nal angle. Adder and shift operations are carried out using these micro rotation angles. Iterations are used to implement the micro-rotations. The required number of iterations is the same as the significant bits that display the rotated components.

There are numerous ways to arrange the CORDIC's iterative equations.

Depending on the number of iterations and the requirements of the application, the user can select and design. The CORDIC can be categorised as follows:

1. Sequential/Iterative Architecture
2. Parallel Architecture
3. Pipelined Design

The CORDIC architectures general classification:

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Although the folded architectures are fundamentally quick and easy, it takes a lot of clock cycles for them to provide the final output for a given input. They are therefore slow. Iterative designs can be unrolled for an n-iteration cycle in unfolded architectures. As a result, they use more hardware resources than folded structures. These designs' rate of computation is:

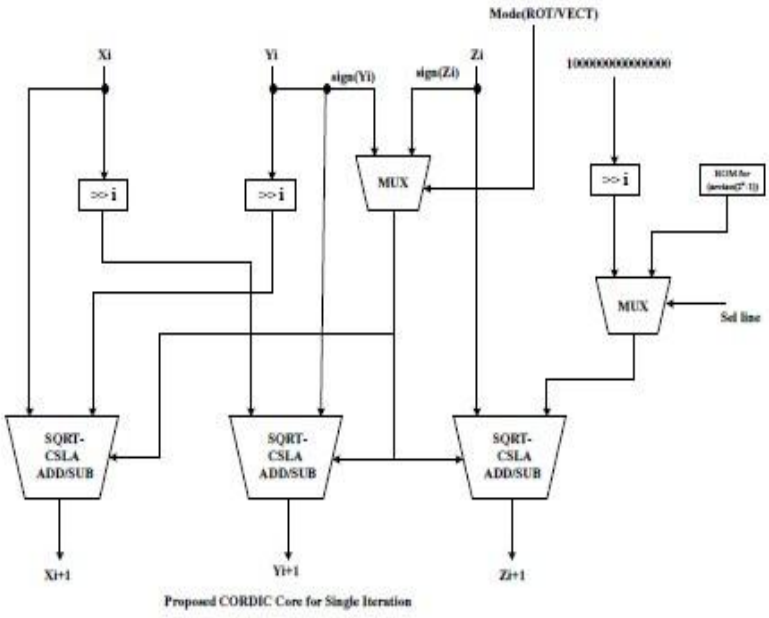


Figure 2: Shows Iterative model

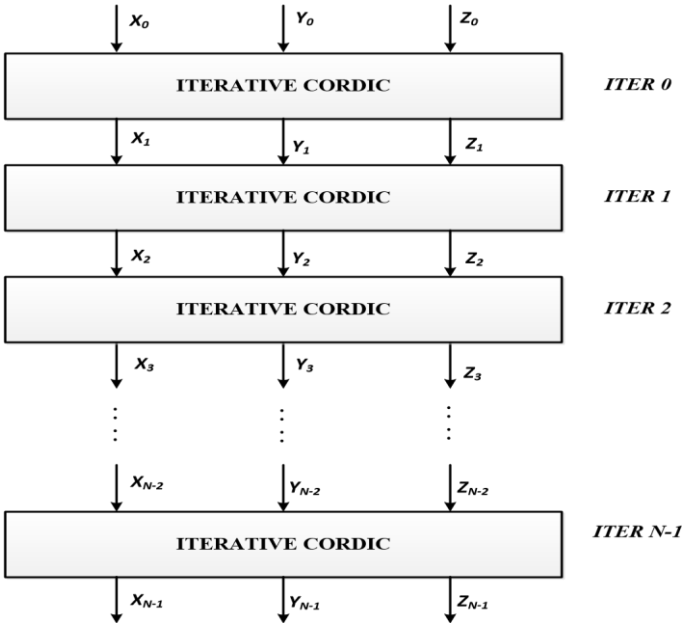


Figure 3: Shows Parallel Model

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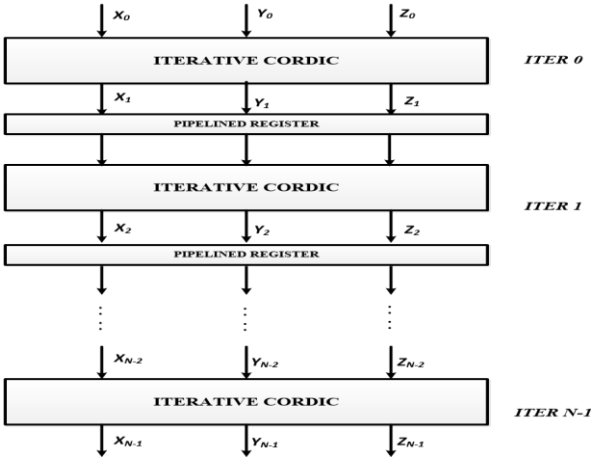


Figure 4: Shows Pipelined model

The parallel and pipelined versions of the unfolded architecture are further separated. The design of the iterative processes in the parallel architectures depicted in Fig.2. At each iteration's subsequent output stages, CORDIC is instantiated numerous times concurrently without the use of any registers, as seen in Fig.3. As a result, the parallel architectures operate less frequently. The parallel architecture and CORDIC's pipelined design are comparable. The pipelined architectures simply differ in that registers are placed at the output stages of each iteration. It runs at a higher frequency than iterative and parallel systems since the maximum delay path is reduced as a result. In Fig.4, the parallel architecture of CORDIC is displayed.

III. SIMULATION AND ASIC SYNTHESIS RESULTS

In this section consists of the simulation waveforms and synthesis results for the various design of CORDIC blocks. The simulation waveforms have been obtained by performing the simulation using Cadence NC Launch tool and synthesis results have been obtained by synthesizing the design blocks through Cadence RC tool using TSMC gpdk 45nm technology. Simulation and synthesis for the pro-posed 16-bit fixed-point iterative, parallel and pipelined CORDIC are shown in area, power and delay of the standard CORDIC (designed by using basic add/sub unit, multiplier for scale factor correction and ROM for all iterations) and Proposed CORDIC are compared . The Proposed Pipelined CORDIC simulation waveform gives output every clock cycle after passing latency of 18 clock cycles for first input for 16 bit CORDIC.

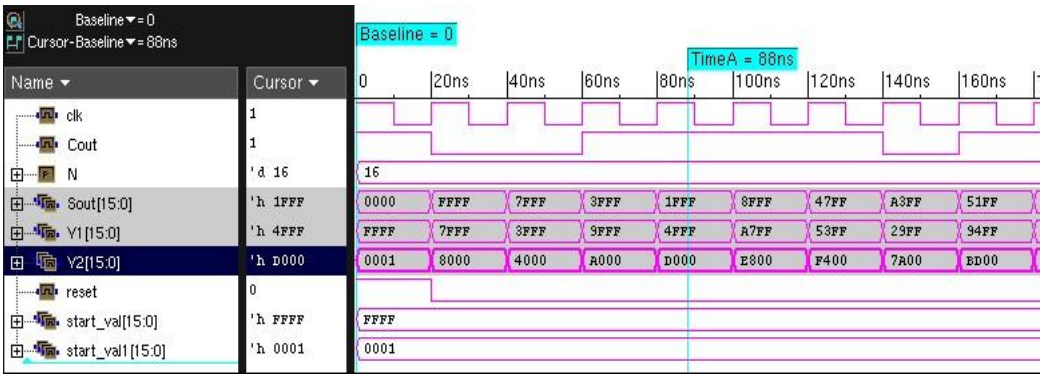


Figure 5: Shows Proposed waveforms

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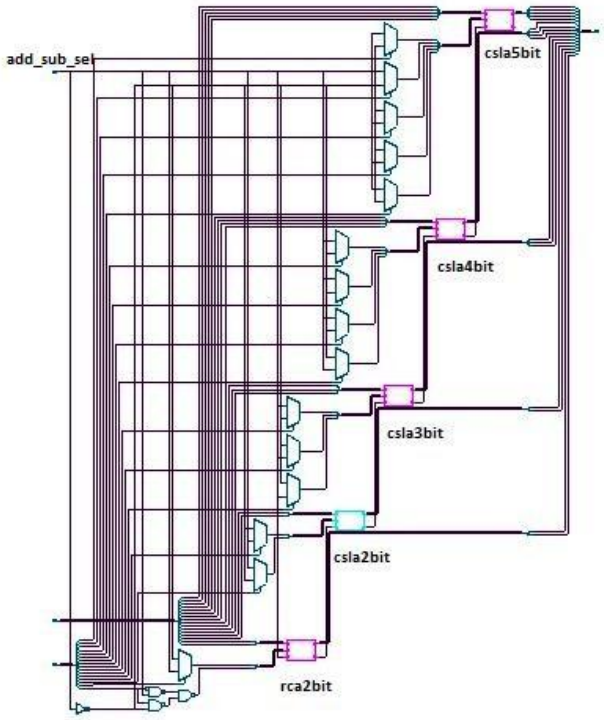


Figure 6: Shows synthesis report

IV. CONCLUSION

We have designed a 16-bit fixed-point iterative, parallel and pipelined CORDIC architectures. This CORDIC can be used for Singular value decomposition. It is favourable for DSP applications as it is designed for fixed-point arithmetic. This architecture consists of the SQRT-CSLA based ADD/SUB unit, which is area, power and delay efficient in comparison.

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