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High Speed Low Area DA Based FIR Filter for Signal Processing Applications

Shaik Imam Valli[1], G.Naga Jyothi[2]
PG Scholar[1], Professor[2]
Department of Electronics and Communication Engineering Golden Valley Integrated Campus Angallu, Madanapalli, Andhra Pradesh, India

ABSTRACT

In this paper, we present a novel Distributed Arithmetic based Finite Impulse Response filter for signal processing applications. DA based FIR filter will occupy more area and power when filter order is increased. To get rid of this, in the paper, we used offset binary coding (OBC) concept. Instead of using binary inputs we are using OBC values for increasing the speed. By using OBC concept the memory usage will be decreased when compared with the basic DA. The proposed design is implemented in Xilinx tool. The area occupied by the proposed design is half when compared with basic DA. The speed of operation of the proposed design is very high.

Keywords: Distributed Arithmetic, Finite impulse response, signal processing, offset binary coding.

I. I.INTRODUCTION

Hearing Aid is an acoustic gadget used to provide clear, amplified and distortion free audio signal which synchronizes with the normal hearing audiogram signal. Abundant signal processing algorithms have been introduced in the hearing aids to get rid of the noise. Hearing aids are of two types. They are analog hearing aid and digital hearing aid. Analog hearing aids convert the input signal to an electrical signal and the digital hearing aids convert the input signal to numerical binary code. Digital hearing aids are more vantage than analog hearing aids because they are more flexible and are self adjustable. The basic operation performed by the digital hearing aid is amplification, filtering, and output limiting [1]. Figure 1a shows the block diagram of advanced the digital hearing aid. Digital Hearing aid comprises of preamplifier, sigma to delta analog to digital (ADC) converter, digital decimation filter and sigma to delta digital to analog (DAC) converter.

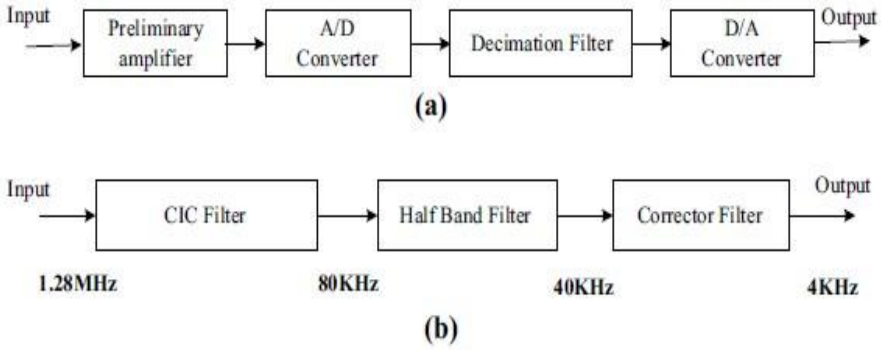


Figure 1: Shows Decimation filter

In the context of aforesaid observations, in this article, we propose a shared LUT OBC DA based FIR filter design in decimation filter. In this article, LUTs are shared by various weights according to the DA input bits. Here the DA input samples are in offset binary code format. The proposed architecture is area and power efficient when compared with existing architectures.

Let us consider the multiplication of two vectors *d* and *x* given by:

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$$y = \sum_{k=1}^{K} d_k x_k \qquad (1)$$

where d_k is fixed coefficient, x_k is the input signal and K is the number of input words. x_K is an N-bit scaled 2's complement binary number such that $|x_k|<1$, and x_k can be expressed as:

$$x_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \qquad (2)$$

$$x_k = \left\{ b_{k0}, \ldots\ldots\ldots b_{k(N-1)} \right\}$$

where b_{kn} denotes N^{th} bit of x_k. By substituting equation (2) in (1), y is given in expanded form as

$$y = \sum_{k=1}^{K} d_k \left[-b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \right] \qquad (3)$$

Equation (3) is the conventional form of inner product expression. By interchanging the summation order, finally we get equation as shown below

$$y = \sum_{n=1}^{N-1} \left[\sum_{k=1}^{K} d_k b_{kn} \right] 2^{-n} + \sum_{k=1}^{K} d_k (-b_{k0}) \qquad (4)$$

Equation (4) gives computation of distributed arithmetic.
Let us consider the summation

$$\left[\sum_{k=1}^{K} d_k b_{kn} \right] \qquad (5)$$

As each b_{kn} can have a value of either 1 or 0, the summation in equation (5) will have only 2^k possible combinations. We can pre-compute all these values and store them in ROM. To accommodate the summation, $\left[\sum_{k=1}^{K} d_k b_{kn} \right]$ ROM must contain the negatives of all the 2^k possible combinations, where b_{k0} in the summation represents the sign bit of the given input. Hence the total size of the ROM will be $2*2^k$. The input value can be applied directly to address the memory as shown in figure (1) and the result i.e. can be stored in the accumulator. After N clock cycles the accumulator contains the result y.

II. PROPOSED SHARED LUT UPDATING OBC DA BASED FIR FILTER

DA is a bit serial operation which is used to compute correlation, convolution and inner products, which are imperative operations present in FIR filters. The significance of DA is its high efficiency of mechanization. In the case of basic DA implementation, when the filter order is increased, the LUT size increases, which affects both area and performance. By using the OBC concept, the LUT size of DA is reduced and performance is increased. Here, instead of binary data (1,0), a signed data (1,1) is used. The OBC DA based FIR filter equation is:

$$x_k = \frac{1}{2} \left[-\left(b_{k0} - \bar{b}_{k0} \right) + \sum_{n=1}^{N-1} \left(b_{kn} - \bar{b}_{kn} \right) 2^{-n} - 2^{-(N-1)} \right]$$

$$S_{(m+rM)n} = b_{(m+rM)n} - \bar{b}_{(m+rM)n}$$

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For large values of 'K' the memory size of DA will be increased eventually. To get rid of this, let the filter order of 'K' is spitted into 'R' vectors such that K = RM. Here 'R' and 'M' can be any two positive integers. Then equation can be rewritten as:

$$y = \frac{1}{2}\sum_{n=0}^{N-1} 2^{-n}\left[\sum_{r=0}^{R-1}\sum_{m=0}^{M-1} d_{(m+rM)}\left[b_{(m+rM)n} - \bar{b}_{(m+rM)n}\right]\right]$$

$$y = \sum_{n=0}^{N-1} 2^{-n}\left[\sum_{k=0}^{K-1} \frac{d_k\,(b_{kn} - \overline{b_{kn}})}{2}\right]$$

we analyze that $S_{(m+rM)n}$ has the input bit sequence which will act as a selection line to the filter coefficient present in the shared LUT register bank.

III. Proposed OBC DA based FIR filter

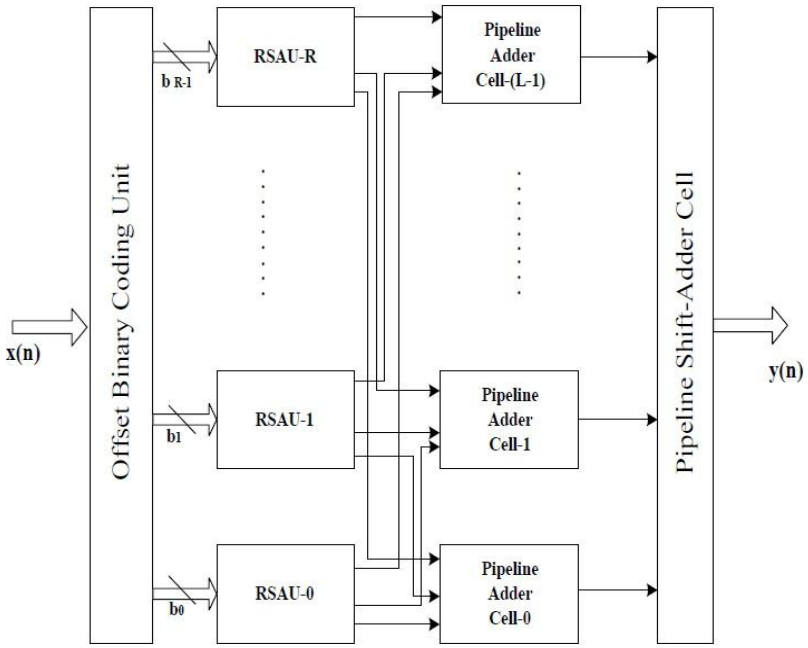


Figure 2: Shows Proposed OBC DA based FIR filter

The proposed shared LUT updating OBC DA (SLU OBC DA) architecture consists of OBC unit, reconfigurable shared LUT updating unit, pipeline shift adder cell, and pipeline adder cell. Fig.2 illustrates the block diagram of SLUT OBC DA based FIR filters. For '*K*' tap filter, let *d*(*k*) be the filter coefficient and *x*(*k*) be the input sample.

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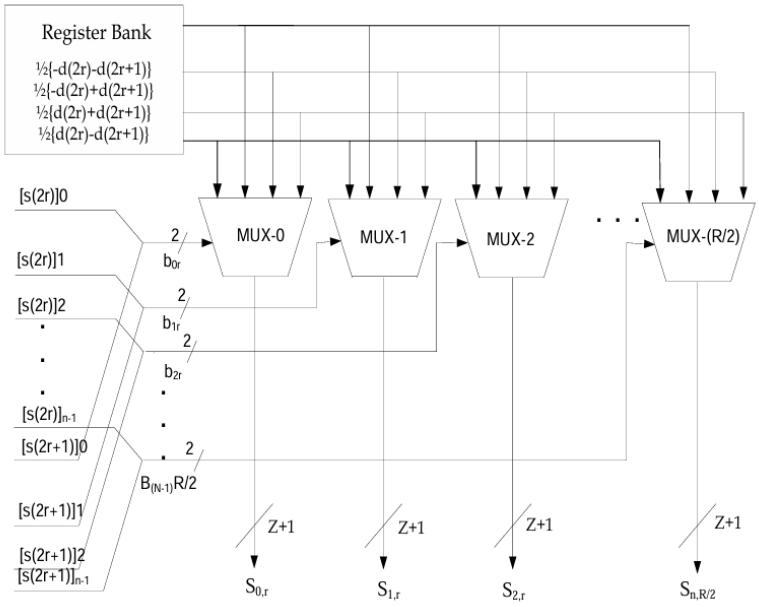


Figure 3: Shows RPPG

The shared LUT DA architecture consists of SIPO shift register unit, reconfigurable partial product generator unit, and pipeline adder tree and pipeline shift adder tree blocks. The block diagram for ASIC implementation of Shared LUT DA based FIR filter is as shown in Fig.3

IV. RESULTS AND DISCUSSIONS

The proposed work is coded in Verilog Hardware Description Language and synthesized by Synopsys ASIC Design Compiler using 90 nm CMOS library. For the 16 tap FIR filter, an 8-bit input data and eight-bit filter coefficients are considered. Area, power delay product (PDP), area-delay product (ADP), maximum sampling frequency (MSF), minimum sample period (MSP) is evaluated. The synthesis results of the proposed SLU OBC DA based FIR filter architecture is compared with the existing DA based pipelined architecture, DA based systolic architecture and rewritable DA based FIR filter architectures. From the synthesis results, it can be noticed that the area occupied by the proposed architecture is very less when compared with the other architectures. The proposed SLU OBC DA based FIR filter occupies 45% less area when compared with the work of [5], 15% less area when compared to the results of Meher [6] and 95% less area when compared with the results of architecture [6] The power consumption of the proposed design is less when compared with other mentioned architectures. The proposed design has less ADP and PDP when compared with that of Meher (2006) and Synposys (2012). The hardware implementation of the SLU OBC based DA FIR filter is carried out on the Xilinx Virtex 5vsx95t-1ff1136 FPGA device. The no. of slice registers (SREG),the no. of slice LUTs (SLUT), the slice delay product(SDP), MSP, MSF, number of slices (NOS) are tabulated in Table.1. The proposed design has 50% less number of SREG

V.CONCLUSION

In this paper, a reconfigurable SLU OBC DA based FIR decimation filter for digital hearing aid application has been proposed. By using the OBC concept and SLU updating scheme, the throughput rate of the proposed architecture is improved. The area complexity of the proposed design is drastically reduced by SLU technique, where the coefficients in the register bank are divided into vectors of smaller bit length for different bit slices. The proposed design has 40% less ADP when compared with the existing designs. It is implemented on FPGA Virtex 5vsx95t-1ff1136 and these results show that the design utilizes 15% less number of slices than the existing designs. From the results, it is evident that the proposed decimation filter will give a cost effective solution for the hardware implementation of the hearing aids.

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