ISSN: 2582 - 6379
Orange Publications
International Journal for Interdisciplinary Sciences and Engineering Applications
IJISEA - An International Peer- Reviewed Journal
2022, December, Volume 3 Issue 4
www.ijisea.org

High Speed Low Power Pre-Charge CAM Design using Hybrid self-control

K. Navyatha[1], G.Naga Jyothi[2]
PG Scholar[1], Professor[2]
Department of Electronics and Communication Engineering Golden Valley Integrated Campus Angallu, Madanapalli, Andhra Pradesh, India

ABSTRACT

In this paper, we present a novel content addressable memory (CAM) is discussed. Although it uses more power, content-addressable memory (CAM) is a popular piece of hardware for highspeed lookup searches. Traditional NOR and NAND match-line (ML) architectures experience charge and short circuit path sharing during pre-charge, respectively. The pre-charge-free CAM that was recently proposed has a high search cost. delay and excessive power consumption of the subsequently proposed self-controlled pre-charge-free CAM. In order to decrease search delay and power consumption, the hybrid self-controlled pre-charge-free (HSCPF) CAM architecture presented in this study employs a unique charge control circuitry. Both the present and planned CAM ML designs were created using the CMOS 45nm technology node and a 1 V supply voltage. When compared to, simulation results demonstrate that the suggested HSCPF CAM-type ML design effectively reduces power consumption and search latency.
Keywords: Content Memory Address, hybrid model, Precharge phase.

I. INTRODUCTION

Using a match-line sense amplifier, a single clock cycle [1, 2] delivers the address of the matched data (MLSA). For all high-speed applications, including radix trees [3], image processing [4], 5G communication networks [5], mobile devices [6], IP routing [7], grey coding [8], and others, the CAM's parallel search strategy outperforms software-based search methods. CAM's parallel hardware activity performs well but uses a lot of power. Consequently, it becomes difficult to design the CAM for lower power consumption and greater performance. One CAM word is created by a row of CAM cells. As seen in Figure.1, each CAM word is associated with a single match-line (ML). All of the MLs are pre-charged to the search operations. Pre-computation-based CAM (PB-CAM) memory organization consists of CAM memory, a smaller parameter memory, and a parameter extractor (PE) (PM). The circuit PE, It takes the input data and derives a parameter (the user's word count) from it. Two steps make up the searching process. The extracted parameter is initially compared to the information in PM. Only the words in the CAM that meet the search criteria will be enabled. The comparisons in the first section are smaller since parameter memory is less extensive than CAM memory. In a similar vein, only the matched data are used for comparisons in the second section. Therefore, PB-CAM takes advantage of the decrease in comparisons and lowers power usage.

Short circuit (SC) power consumption in traditional NOR CAM was addressed by the authors in [16], who also created a precharge-free (PF) CAM that removes the SC current route during precharge m ismatch circumstance. Although PF CAM similarly prevents the charge sharing of NAND CAM cells, its performance is hampered by a series chain of MLs. Self-controlled precharge (SCPF) CAM ML, where output control is based on the charge at each CAM cell node, was invented in [17] to further enhance the performance of the PF CAM architecture. Performance was improved with this design, but at the expense of power usage. In this paper, we attempted to develop a new precharge-free CAM ML architecture, hybrid, to address the shortcomings of PF CAM and SCPF CAM.

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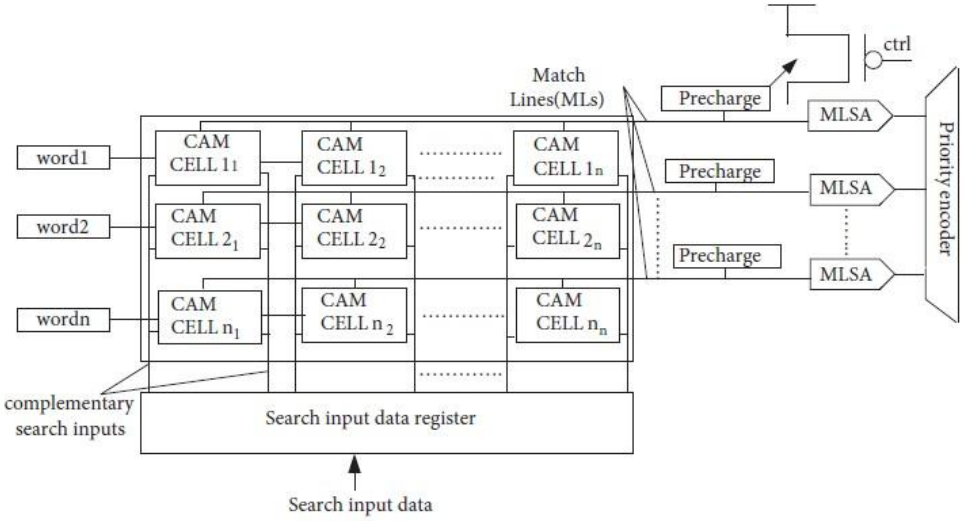


Figure 1: Shows Basic CAM

II. NOR MATCH LINE

NOR ML architecture is created by parallel connections between CAM cells. In order to create comparison circuitry in NOR CAM cells, four NMOS transistors are necessary. M1 and M2 transistors' gates are linked together in series to Figure 2 illustrates the SRAM cell's differential storage bits D and Dbar. Differential search bits SL and SLbar are coupled to transistors M3 and M4's gates. ML precharges to a high voltage through transistor P1 regardless of the search input or the stored data in the memory when precharge control signal ctrl is low. The ML output depends on the search input and bits stored in the CAM cells when the control is high during evaluation. If an input search finds matches for every bit in a row.

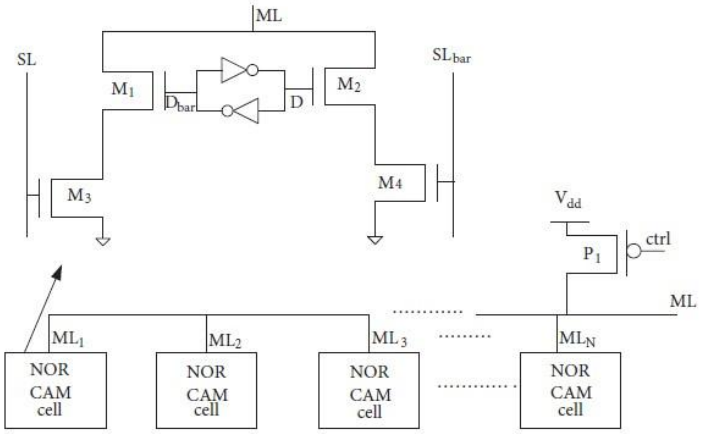


Figure 2: Shows NOR CAM

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Table 1. Truth table for NOR CAM cell.

SL	D	ML	Output indicates
0	0	Match	High
0	1	Miss	Low
1	0	Miss	Low
1	1	Match	High

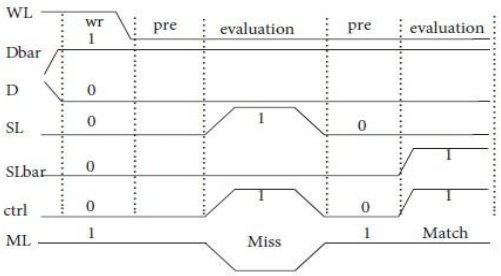


Figure 3:Shows Timing diagram Architectures for CAM without precharge

The majority of the efforts published thus far have focused on power switching, whereas PF CAM and SCPF CAM have focused on electricity short circuit. It has been determined that the short circuit current in the NOR CAM during ML precharging causes a higher power consumption.

III. PROPOSED WORK

The proposed HSCPF CAM cell has a two 6T SRAM cells and four NMOS transistors (M7, M8, M17, and M18) architecture. Two successive CAM cells are controlled by a hybrid charge control circuit. According to Fig.4, it consists of M9 and M10 transistors. In this charge control circuit, the charge values at nodes S0 and S1 regulate the ML output for high or low. Connected to node S1, while the source of the M10 transistor is connected to node S0. If the search input matches the pre-stored data in two CAM cells, the charge value at nodes S0 and S1 is high, which then passes a high signal. According to Figure 13, all of these CAM words are linked together in parallel to form an ML structure. The charge values at the nodes will change if the search content matches the pre-stored data in the first CAM word. High S0 and S1 values. Up until nodes SN1 and SN, this procedure is carried out for the remaining CAM words in the ML structure. The ML associated with a word charges excessively if all of the pre-stored bits in that word match the input search phrase. The ML associated to that word costs too little when pre-stored bits in a word are not even slightly matched with the input search word.

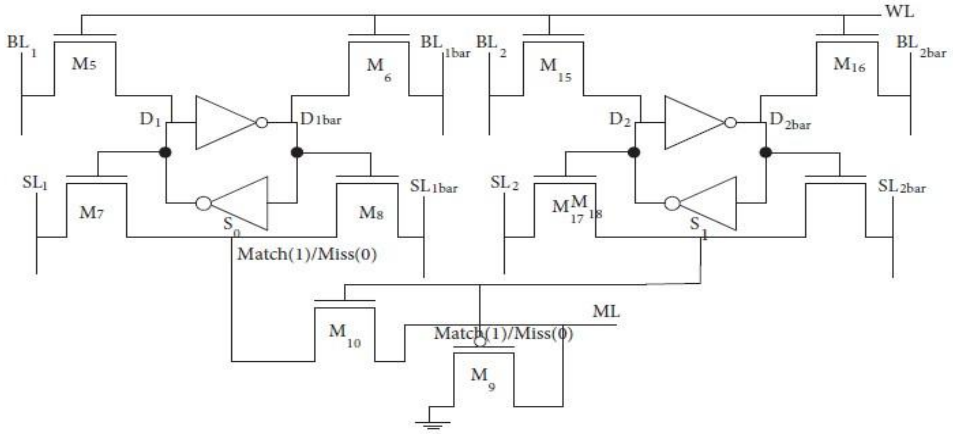


Figure 4: Shows HSCPF CAM cell

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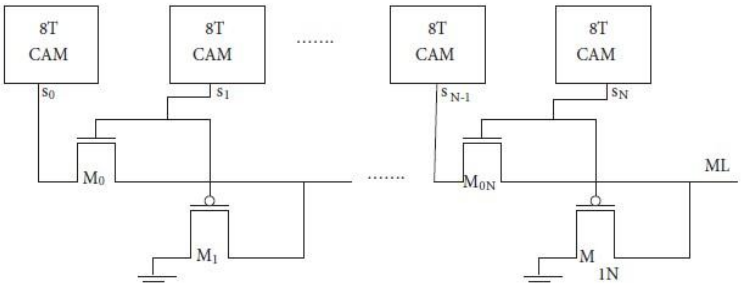


Figure 5: Shows Match line architecture of HSCPF

IV. SIMULATION RESULTS

The suggested HSCPF CAM design, which has an 8-word, 8-bit size, is implemented in the 45-nm technology node using the generic process design kit (GPDK), and simulations are run using the Virtuoso tool for validation. Basic NAND- and NOR-type ML CAMs, precharge-free CAMs of [6] and [7] of size 8 8, and the suggested design are all included in the simulation. The power, search delay, and energy-metric of these designs are contrasted with those of the suggested design. Figure 15 displays a partial layout perspective of the suggested CAM cell design. This is verified in Cadence Virtuoso for DRC and LVS check. Due to the charge management circuitry being shared by two subsequent CAM cells and the usage of folding and chaining transistors during layout, the HSCPF CAM design has a smaller area than other standard CAM designs.

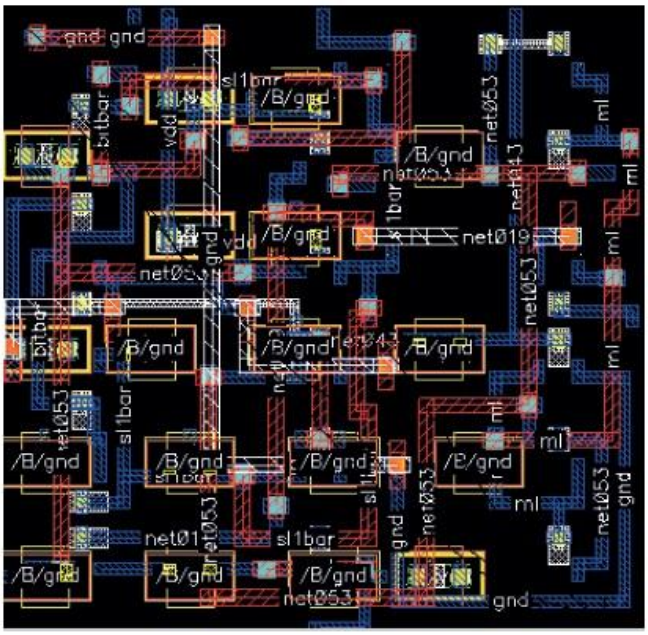


Figure 6: Shows Layout Diagram

V. CONCLUSION

A low energy-metric HSCPF CAM design is presented in this research. The improved charge control circuitry of the proposed design can be shared by two subsequent CAM cells, significantly lowering the number of transistors needed for the charge control circuitry. At 45nm technology node CMOS process with 1 V supply voltage, the suggested ML architecture is simulated for various process corners and MC simulations. When compared to PF CAM and SCPF CAM, the suggested design considerably reduces search delay, power, as well as energy metric since it features charge control circuitry with less transistors than SCPF CAM.

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