ISSN: 2582 - 6379
Orange Publications
International Journal for Interdisciplinary Sciences and Engineering Applications
IJISEA - An International Peer- Reviewed Journal
2022, December, Volume 3 Issue 4
www.ijisea.org

A Novel High Speed Low Area Booth Multiplier

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ABSTRACT

This work introduces an 8*8 Booth multiplier with enhanced power, delay, and area performance. An addition of encoded partial products in a parallel structure is the main adjustment for lowering delay. An improved B2C architecture, an improved Booth encoder, and a special square root carryselect adder with carry-look ahead adder logic to reduce multiplier delay are other improvements. Comparing this design to recently published similar designs, it obtained reductions in power consumption of 26.6%, area usage of 15%, and data arrival time of 25.6%. All of the suggested circuits were created using 32 nm CMOS technology from Synopsys.
Keywords: Multiplier, booth algorithm, adder, power consumption

I. INTRODUCTION

In signal processing techniques like the fast Fourier transform (FFT), finite impulse response (FIR), infinite impulse response (IIR), and audio/video codecs, multipliers are one of the essential building blocks. Multipliers with high performance and small form factors are crucial because portable wireless devices like smart phones, laptops, tablets, and PCs require signal processing algorithms. Multiplication can be implemented using a variety of methods, but practically all of them rely on the fundamental AND operation for bit-by-bit multiplication and partial product addition utilizing full adders and half adders. A multiplier's delay is mostly determined by the quantity of partial products and the adder operation used to produce the sum. Fig.1 depicts the standard Booth multiplier architecture for a radix-4 8*8 implementation. With 15-bit adders/subtractor, radix-4 Booth encoders, and radix-2 multipliers in each level, the number of partial products is decreased from 8 to 4 as compared to a conventional radix-2 multiplier. A method of encoding that takes into account groups of the multiplier's three bits is used to create the partial products with multiplicand X and multiplier Y.

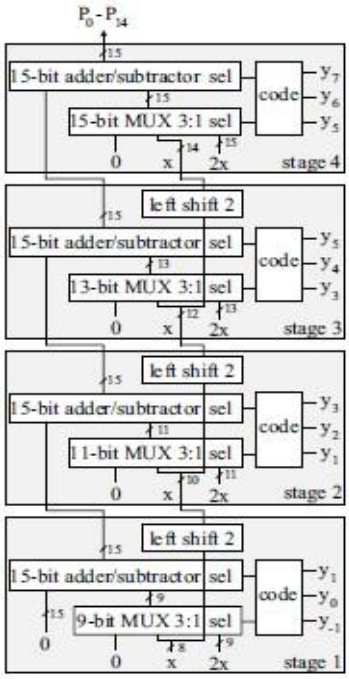


Figure 1: Shows Booth Multiplier

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II. PROPOSED BOOTH MULTIPLIER

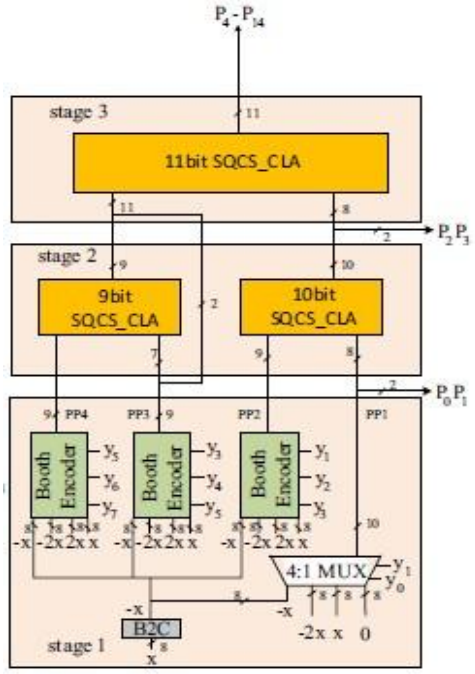


Figure 2: Shows Proposed Design

In contrast to series addition of partial products, our proposed two-stage radix-4 8-bit Booth multiplier is created in this study using parallel addition. This has a significant impact on the decrease in delay. Fig. 2 shows the specifics of the proposed parallel architecture. The two adders of the first stage are concurrently fed with each of the four partial products (PP1 to PP4), and they work in tandem. The worst path delay for this 8-bit multiplier is highlighted in Fig. 2 and goes from "B2C," through "Booth Encoder," through "10b SQCS CLA," of the first stage addition, to the final "11b SQCS CLA." When compared to standard radix-4 8-bit multipliers [6, 8–10, 12], this structure saves two addition stages, and when compared to existing designs, it saves one addition stage. The suggested radix-4 8-bit Booth multiplier makes use of the SQRT CSA with CLA logic (CS-CLA). The final total bits are selected depending on the real carry in, and it simultaneously conducts the addition operation for both carry-in as logic "0" and "1". The first step of the partial sum addition does not have a carry-in for the two parallel adders.

III. COMPARISON RESULT

Using 32 nm CMOS technology, the proposed Booth multiplier and the multiplier in [3] were created using the Synopsys design compiler (DC). The suggested multiplier's layout was also completed. Input and output registers with a clock frequency of 500 MHz and a supply voltage of 1.05 V are included in the overall power and area. Based on schematic circuits that were specifically designed, the 90 nm design resulted in [3]. Table 3 compares the performance of the suggested Booth multiplier to that of [2,3]. Results for delay, area, and power are displayed for [2] using formula (5) from [2], which normalizes the data to CMOS 32 nm technology with 1.05 V supply voltage. The post-layout outcomes solely apply to the core. The proposed radix-4 8-bit Booth multiplier's post-layout results in improvements in delay, total power, and efficiency of 24.6%, 21.5%, and 28.7% compared to the approximate Wallace-Booth multiplier in [2] for the area delay product. When compared to the Booth multiplier in [3], the suggested design's synthesis results show a 25.6% improvement in delay, a 15% reduction in area, a 26.5% power savings, and a 36.8% improvement in area delay product.

IV. CONCLUSION

In contrast to existing Booth multiplier designs, the architecture given in this work is a novel radix-4 8-bit Booth multiplier. A two-stage parallel addition of partial products as opposed to a sequential four-stage addition, a unique

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SQRT CSA with CLA logic for adder implementation, a B2C optimization with bubble pushing techniques, a Booth encoder optimization with bubble pushing techniques are the main advancements over the current designs. Reduced area and power are further benefits of these design enhancements. In comparison to recently released ASIC Booth multiplier designs, this design produces exceptionally low area delay and power delay products when paired with the delay enhancements.

REFERENCES:

[1] V.B.P. Biradar, G. Vishwas, C.S. Chetan, Design and performance analysis of modified unsigned braun and signed Baugh–Wooley multiplier, in International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (2017).
[2] N.V.V.K. Boppana, S. Ren, A low-power and area-efficient 64-bit digital comparator. Circuits Syst. Comput. **25**(12), 1650148–1650163 (2016)
[3] A.R. Cooper, Parallel architecture modified Booth multiplier. IEE Proc. G Electron. Circuits Syst. **135**(3), 125–128 (1988)
[4] G. Divya, A. Amonkar, Design and implementation of high speed modified Booth multiplier using hybrid adder. Comput. Methodol. Commun. (2017).
[5] F. Elguibaly, A fast parallel multiplier—accumulator using the modified Booth algorithm. IEEE Trans. Circuits Syst. **47**(9), 902–908 (2000)
[6] Y. He, Z. Zhang, A low-error energy-efficient fixed-width Booth multiplier with sign-digit-based onditional probability estimation. IEEE Trans. Circuits Syst. **65**(2), 236–240 (2018)
[7] S.R. Kuang, J.P. Wang, Design of power efficient configurable Booth multiplier. IEEE Trans. Circuits Syst. **57**(3), 568–580 (2010).
[8] Manjunath, V. Harikiran, K. Manikanta, S. Sivanantham, K. Sivasankaran, Design and implementation of 16 × 16 modified booth multiplier, in International Conference on Green Engineering and Technologies (2015).



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