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A Normal i/o order Radix 2 FFT architecture to process Twin data streams for MIMO

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ABSTRACT

This work introduces a simultaneous computing of many independent fast Fourier transform (FFT) operations with their outputs in natural order is necessary for many applications nowadays. Consequently, this brief demonstrates a brand-new pipelined FFT processor that can compute the FFT for two separate data streams. The multipath delay commutator FFT architecture serves as the foundation for the suggested architecture. To handle the odd and even samples of two data streams separately, it has a N/2-point decimation in time FFT and a N/2-point decimation in frequency FFT. The bit reversal operation is performed by the shift registers in the FFT architecture by interleaving the data. Therefore, the proposed architecture requires a lower number of registers and has high throughput.
Keywords: Bit reversal, fast Fourier transform, decimation in time, decimation in frequency

I. INTRODUCTION

One of the most often utilised processes in wireless communication applications, such as Wideband, terrestrial digital video broadcasting, orthogonal frequency division multiple (OFDM) accesses, and signal processing applications are also included. Single-path delay feedback (SDF) and multipath delay commutator (MDC) are widely used in a family of pipelined FFT systems that are explained in [1]. There are applications where more than one data stream needs to be processed, including image processing, array signal processing, multiple-input multiple-output OFDM, and others. To produce the outputs in natural order, multiple FFT processes must be performed simultaneously, and a special bit reversal circuit is also necessary. FFT designs [2] are capable of handling several independent data streams. However, in [2] and [5], a single FFT processor handles the processing of all the data streams. [5] processes each of the four different data streams separately. In [2], eight data streams are similarly processed over two domains. As a result, it is not possible to access multiple data streams' outputs simultaneously. Multiple FFT processors must be used in order to process the data streams simultaneously. In [3], one to four data streams are handled for a wireless local area network application using various data routes. In [4], data from various data streams are interspersed to process them simultaneously. The architectures in [2]–[4] do not, however, have any particular bit reversal circuit. A few circuits are suggested in [6]–[9] to restore the bit- reversed FFT output to its original order. The bit reversal circuits are suggested in [8] for various radices. For variable length FFT, whose register complexity is N, a similar structure is suggested in [9]. Bit reversing the data from the pipelined FFT design is possible with these circuits.

II. PROPOSED DESIGN:

Fig.1 illustrates the concept of computing an N-point FFT using two N/2-point FFT operations and an additional stage of butterfly operations; the architecture is not illustrated, but the methodology is. Simply stating that N/2 even samples (x(2n)) are reordered after the N/2-point DIF FFT operation and N/2 even samples (x(2n)) are reordered before the N/2-point DIT FFT operation is all that the reordering blocks in Fig.1 are intended to convey. A further one step of butterfly operations is applied to the outputs of the two N/2-point FFTs in order to compute the N-point DIT FFT from those results. As a result, the outputs produced by a later butterfly stage are in chronological order.

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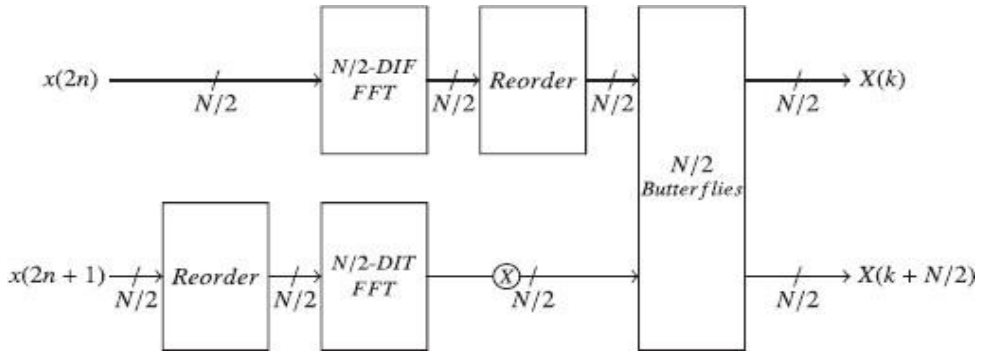


Fig.1.Proposed design

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III. SYNTHESIS RESULTS:

Although a number of architectures [2]–[5] are suggested for processing multiple independent data streams, not all streams are processed by a separate FFT processor at once. Furthermore, the architecture in [5] has drawbacks, such as poor throughput per data stream and the requirement for challenging dual port RAMs. Given that the suggested design handles two streams (NS = 2), the computation complexity of the architecture [5] shown in Table IV correspond to two streams. If two or more streams need to be processed using the single stream architectures [6], [7], then two or more of these architectures are needed in simultaneously. The suggested architecture's critical route is 2TMUX+TA+TM (the path along SW, SW1, and processing element). Given that the multiplexers in the reordering circuit are wired in series, the critical route may be dependent on bit reversal circuits if N is big. The suggested design can process two data streams simultaneously and has two N-point FFT structures. As a result, the suggested architecture's complexity is normalised to a single data stream, producing two log2 N + 2 adders, three log2 N 2 registers, and two log2 N 2 multipliers.

FPGA IMPLEMENTATION RESULTS

N	Registers	LUTs	DSP48Es	Latency	Throughput
256 [7]	1038	1594	28	937ns	720MS/s
512 [7]	1186	1824	32	1889ns	720MS/s
256 [8]	968	1178	28	1263ns	380MS/s
512 [8]	1126	1497	32	2568ns	380MS/s
256 Prop.	1536	2420	56	505ns	1520MS/s
512 Prop.	1728	2952	64	1010ns	1520MS/s
1024 Prop.	1920	4116	72	2021ns	1520MS/s
2048 Prop.	2112	5662	80	4042ns	1520MS/s

Table.1 FPGA Implementation

IV. CONCLUSION:

An innovative FFT processor with outputs produced in the natural order has been discussed in this short. The suggested processor is ideal for many high-speed real-time applications since it can handle two separate data streams concurrently. By merging two FFT processors, the bit reversal circuit that was present in earlier designs is eliminated. The architecture's registers are still utilized. As a result, there is no need for extra registers to bit-reverse the outputs. Additionally, compared to earlier architectures, the suggested architecture offers a better throughput. The suggested FFT processor is superior in terms of hardware complexity and performance thanks to these characteristics.

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