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Memory based FIR filter for ECG applications

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ABSTRACT

Finite Impulse Response (FIR) filters play a key role to remove the noises present in the ECG signals. Generally adaptive filters will contain multipliers, adders and shift registers. Multipliers will occupy more area and power consumption To get rid of this we go for multiplier less architecture. Distributed Arithmetic architecture is the one which is more useful for higher order filters. In this we are going to use Xilinx synthesis tool for getting area power and speed. Therefore, the proposed architecture requires a lower number of registers and has high throughput. Keywords: filter, ECG signals, adaptive filter, area, power, speed
Keywords: Finite Impulse Response (FIR) Filter; Electrocardiogram (ECG); Distributed Arithmetic (DA); Memory-Less Architecture; Adaptive Filtering; Low-Power Design; Enhanced 4:2 Compressor.

I. INTRODUCTION

In signal processing and control applications where the signals and transfer functions involved are time invariant and known at design time, designing fixed filters and controllers to achieve the desired design goals is sufficient. In many applications, however, signals, transfer functions, and the environment in which the system operates are time varying. In some applications, such as in active noise and vibration control, it is the rule rather than the exception that the system to be controlled is unknown at design time. In such situations a self-designing or self-adjusting filter/controller is necessary to achieve the desired system function in a changing environment. Self-adjusting filters, better known as adaptive filters, might have any underlying filter structure. The most widely used adaptive filter structure is the transversal structure due to the stability and simplicity of analysis of those filters. The linear combiner structure is a generalized version of the transversal structure, and is mainly used in array signal processing applications. Recursive adaptive filters have also found wide application in adaptive line enhancers, autoregressive signal modelling and channel equalization. A third structure, which is widely used in adaptive linear prediction applications, is the lattice structure[1-3].

In the statistical approach to the solution of the linear filtering problem, we assume the availability of certain statistical parameters (i.e. mean and correlation functions) of the useful signal and unwanted additive noise, and the requirement is to design a linear filter with the noisy data as input so as to minimize the effects of noise at the filter output according to the statistical criterion. A useful approach to this filteroptimization problem is to minimize the mean-square error value of the error signal defined as the difference between some desired response and the actual filter output. For stationary inputs, the resulting filters solution is commonly known as the WIENER FILTER, which is said to be optimum in the mean square error sense. A plot of mean-square value of the error signal versus the adjustable performance of linear filter is referred to as the error-performance. The minimum point of this surface represents the WEINER SOLUTION.

II. PROPOSED DESIGN:

The proposed Memory-less DA (MLDA) filter architecture is explained in this section. It consists of 2:1 multiplexers instead of memory elements, and the adders of memory less DA architecture are replaced with enhanced 4:2 compressor as shown in Fig.1. MLDA consists of serial in parallel out shift register (SIPOSR), four 2:1 multiplexers, and enhanced 4:2 compressor adders. The input data x_k is fed to the SIPOSR and is given as one of the input of the 2:1 multiplexer and the other input of the multiplexer is the logic '0'. The selection lines for four 2:1 multiplexers are the filter coefficients. If the selection input line is high, then filter input will present at output else the output of multiplexer is zero. The outputs from multiplexers are given to the enhanced 4:2 compressor adder[3-5].

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The enhanced 4:2 compressor adder is designed with dual mode logic (DML). DML logic consists of XOR/XNOR module and MUX module. The XOR/XNOR module is developed with CMOS logic and MUX module is developed using transmission logic gate (TG). By using DML realization, we can achieve better results in area and power. The A_1 and A_2 inputs are fed to XOR/XNOR1 module and A_3 and A_4 are fed to XOR/XNOR2 module. The outputs from XOR/XNOR modules are given to the MUX1 module with A_4 as a selection line. The outputs from MUX1 module are given as inputs to the MUX2 module with A_5 as selection line to generate sum. To achieve carry, A_4 and A_5 are given to MUX3 with selection line as one of the output of MUX2. Finally from MUX3 and MUX4 we get sum and carry output.

The proposed MLDA is implemented in Adaptive FIR filter. Arithmetic performance of higher order adaptive filters is so complex, so higher order filters are decomposed into smaller order adaptive FIR filter which makes the design implementation simple.

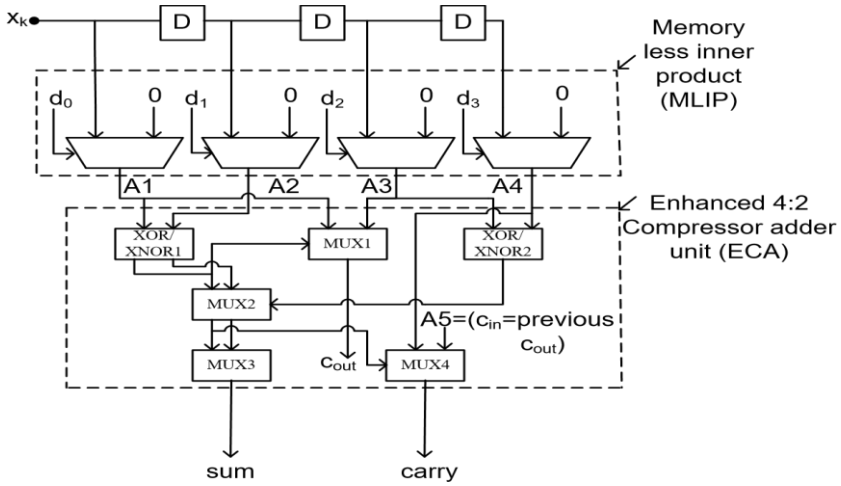


Fig.1.Proposed MLDA architecture

2.1. Proposed MLDA for smaller order adaptive FIR Filter:

In this section, the proposed design is implemented for filter order K=4 and is shown in Fig.2. The proposed design consists of Memory Less DA block (MLDA), weight increment block (WIB), signmagnitude separator and control word generator block. The MLDA block consists of memory less inner product block (MLIP) and enhanced 4:2 compressor adder (ECA) block. The input X (k) is given to the MLIP block, the MLIP block consist of four 2:1 multiplexers, one input of 2:1 multiplexer is input signal and other input is logical '0' shown in fig.2. The selection lines for four multiplexers are the filter coefficients which are taken from the weight increment block. The four outputs from MLIP are A_1, A_2, A_3, and A_4 are given to ECA. A_5 is the fifth input to the compressor which is the C_{out} of the previous stage compressor. The four inputs A_1, A_2, A_3, A_4 and sum output will have same weights and finally ECA obtain sum and carry. The generated sum and carry are added to obtain final filter output y(k). Obtained filter output y(k) is subsequently subtracted from the desired signal D(k) to achieve error sample e(k)[6-7].

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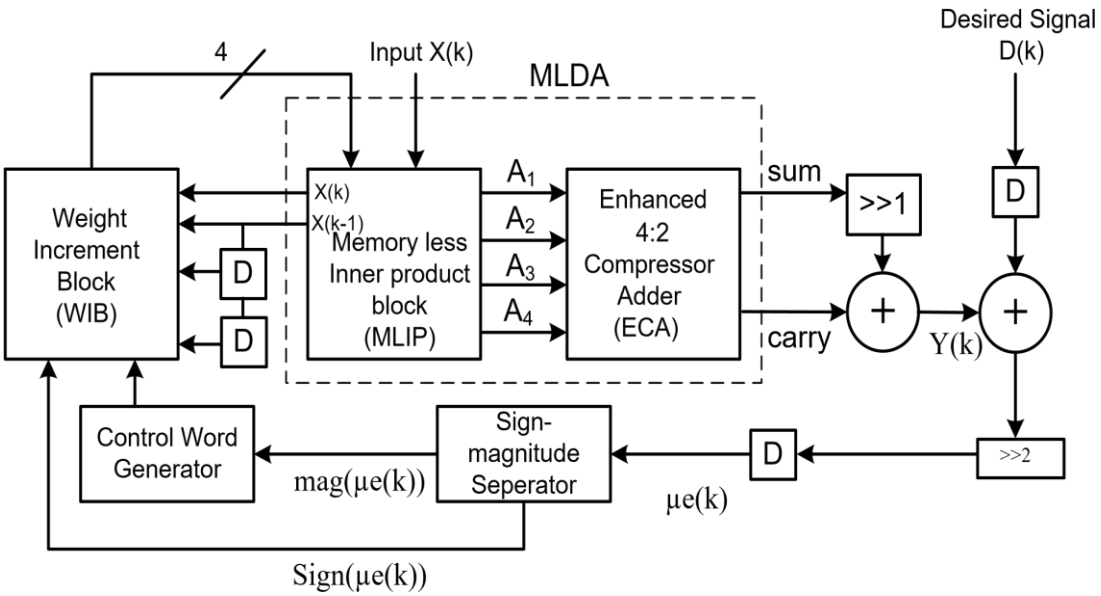


Fig.2 Four tap adaptive FIR filter using MLDA

The input data X(k) is fed to the three D-ff and produces the signals of X(k-1),X(k-2) and X(k-3) signals which are given to the weight increment block (WIB). It consists of four barrel shifters, four adder/subtractor units, four delays and a word parallel bit serial converter. The barrel shifter shifts the different input values *xk* for k =0, 1, . . .,$K-1$ by appropriate number of locations according to the control signal 't'. The barrel shifter obtains the required increments to be added with or subtracted from the present filter coefficient values. The sign bit of the error is used as the control for adder/subtractor unit. When sign bit is zero the barrel-shifter output is respectively added with the present filter coefficient else it is subtracted from the content of the corresponding present filter coefficient value in the weight register and are passed to word parallel bit serial converter. The output 'A' from WIB are given as selection lines for the four 2:1 multiplexer's of the memory less inner product block.

III. SYNTHESIS RESULTS:

Power, Area and timing have been estimated for the proposed design and comparative analysis is done with the existing architecture. The proposed design contains only four multiplexers in place of LUT, which is the main concern for area complexity. Multiplexers in the proposed design reduces the area significantly, moreover the compactness of the enhanced compressor adder gives an extra advantage to reduce the size of the filter more than 50%.The existing model and the proposed design has been coded in Verilog HDL and synthesized in Xilinx software for filter tap of K=16, 32 and 64 to compute the area, delay and power. From the synthesis result, it is clearly observed that the proposed design offers 52.79% less area and 36.50% less ADP when compared with pipelined DA based adaptive FIR filter. 69.25% power reduction and 35% of PDP compared with the existing model and are tabulated in Table. 1.

Design	Filter Length, K	MSP* (ns)	Throughput (per μs)	Area (sq. μm)	Power (mW)	ADP* (sq.um x ns)	PDP(mW X ns)
Park[11]	16	7.09	141.04	88719	2.917	629617.71	20.68153
	32	8.31	120.33	177460	5.834	1474692.60	48.48054
	64	9.6	104.167	364820	11.67	3502272.00	112.032
Proposed	16	11.8	84.745	41946	1.33	494962.8	15.694

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Design	32	12.05	82.987	85262	1.695	1027407.00	20.42475
	64	13.11	76.278	170678	3.2548	2237588.58	42.6704

Table.1 Synthesis results

IV. CONCLUSION:

We have explored different ways to improve the performance of adaptive filters. A LMS algorithm, which we called the Least Mean Square algorithm with Orthogonal Correction Factors, was proposed. The proposed algorithm provides faster convergence than the widely used LMS A balanced realization is known to minimize the parameter sensitivity as well as the condition number for Grammians. Furthermore, a balanced realization is useful in model order reduction.

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