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Advanced VLSI Technique for Error Detection and Correction in Space Systems

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ABSTRACT

This study introduces a novel approach to error detection and correction within Very Large-Scale Integration (VLSI) systems, specifically tailored for space applications. The core of this research is the development and implementation of a sophisticated 2-dimensional error correction code designed to significantly enhance memory reliability in the harsh conditions of outer space. Traditional error correction methods, while effective to a certain extent, fall short in addressing the complex phenomenon of burst errors—errors that occur in multiple bits simultaneously as a result of a single disruptive event, such as cosmic radiation. The proposed error correction scheme innovatively employs extended XOR operations, covering larger blocks of data, thus offering a more comprehensive solution for detecting and correcting burst errors. Moreover, the integration of Cyclic Redundancy Check (CRC) techniques further bolsters the error detection and correction capabilities of the system. Through a detailed comparison with existing methods, our study demonstrates that the proposed 2-dimensional code not only addresses the limitations of current error correction techniques but also contributes to the advancement of memory system reliability in space engineering. The implementation of this method is poised to provide better performance in environments where burst errors are prevalent, marking a significant step forward in the domain of space system design and reliability.

Key words: Error detection, Error correction, Cyclic Redundancy Check (CRC), XOR operations, burst errors, Space engineering, VLSI systems.

I. INTRODUCTION

A. Background and Motivation for the Study

The relentless advancement in space exploration and satellite technology necessitates robust Very LargeScale Integration (VLSI) systems that can withstand the unforgiving conditions of outer space. A critical aspect of these systems is the reliability of on-chip memory, which is increasingly vulnerable to bit errors due to environmental factors such as cosmic radiation, alpha and neutron particles, and extreme temperatures [1]. These bit errors can lead to data corruption, significantly undermining the integrity and reliability of space missions. Traditional error detection and correction techniques, although effective in many scenarios, are not fully equipped to handle the unique challenges presented by the space environment, particularly the phenomenon of burst errors [2]. Burst errors, characterized by multiple bits flipping simultaneously due to a single event, pose a significant challenge to the efficacy of conventional error correction codes. [3] [4].This vulnerability underscores the need for enhanced error detection and correction techniques tailored specifically for space applications, where the margin for error is minimal, and the cost of failure is astronomically high [5].

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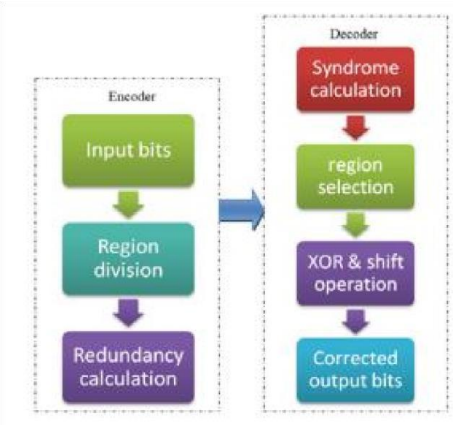


Figure 1: Shows ECC

B. Problem Statement:

The Challenge of Burst Errors in Space Applications

Burst errors represent a formidable obstacle in maintaining the reliability of memory systems in space. Traditional encoder and decoder error correction, designed primarily for single-bit errors or closely located errors, fall short in effectively detecting and correcting burst errors, which can span several bits and are induced by singular high-energy events [6]. This limitation becomes increasingly pronounced with the miniaturization of circuit components and the densification of memory arrays, making existing methods less effective and calling for innovative solutions to safeguard data integrity against such errors [7].

C. Objective of the Paper

This paper aims to introduce a novel error correction technique designed to effectively address burst errors in space applications. By extending XOR operations and incorporating Cyclic Redundancy Check (CRC), the proposed 2dimensional error correction code seeks to enhance memory reliability in the challenging conditions of outer space [8]. This study not only addresses the limitations of current ECC methods in combating burst errors but also sets the stage for a new paradigm in the design and implementation of error correction codes for space engineering [9]. Through rigorous analysis and comparison with existing techniques, this paper demonstrates the superiority of the proposed method in ensuring the integrity and reliability of on-chip memory systems, ultimately contributing to the success and sustainability of space missions [10],[11]

II. LITERATURE REVIEW

Error Detection and Correction (EDAC) techniques have been extensively studied and developed to ensure data integrity and reliability in memory systems. Techniques such as Single Error Correction and Double Error Detection (SECDED) codes have been pivotal in addressing single-bit errors and detecting double-bit errors but are less effective against multiple bit upsets (MBUs) [12].

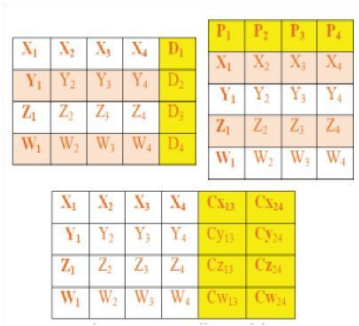


Figure 2: Shows Encoding model.

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Advanced EDAC methods, like those employing Matrix codes, have offered improvements in reliability and cost efficiency for memory chips, demonstrating the capacity to mitigate more complex error patterns [13]. Furthermore, the introduction of Mix codes has shown promising results in mitigating MBUs in fault-secure memories, offering a nuanced approach to error correction that combines the strengths of different coding strategies [14] [16].

A. Limitations of Current Methods in Addressing Burst Errors

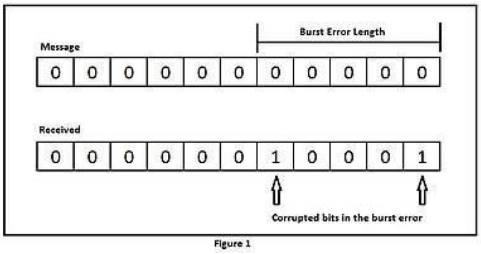


Figure 3:Shows Burst Error

Despite advancements, existing EDAC methods face significant challenges in effectively addressing burst errors, especially in space applications where MBUs are prevalent. Studies have shown that traditional techniques may fail to correct multiple adjacent errors, leading to data corruption [15]. The selection of optimal interleaving distances has been proposed as a mitigation strategy for MCUs, yet this approach does not fully resolve the intrinsic limitations of conventional codes in handling burst errors effectively [17]. This gap underscores the need for innovative coding techniques capable of providing comprehensive protection against such error patterns.

B. Importance of Robust Error Correction in Space Applications

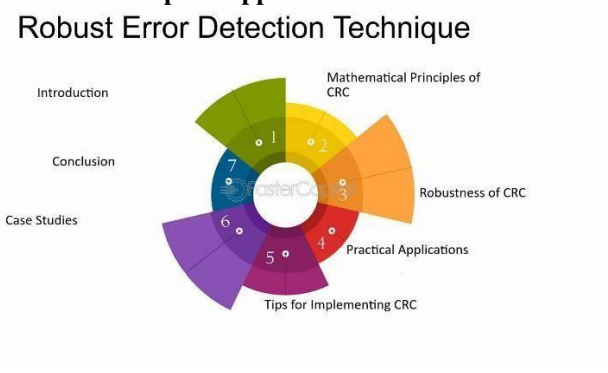


Figure 4:Shows Robust Error Detection technique

The harsh space environment exacerbates the risk of burst errors, making robust error correction a critical requirement for space applications. The development of Fault Secure Encoder and Decoder systems for Nano Memory applications marks a significant step toward addressing this need, offering a framework for enhancing memory reliability against MCUs [18]. Moreover, the study of the effects of multibit error correction codes on memory reliability highlights the urgent necessity for EDAC techniques that can adapt to the evolving challenges of space technology, ensuring data integrity amidst the complex error mechanisms encountered in outer space [19]. New linear SEC-DED codes with reduced triple error miscorrection probability further illustrate the ongoing efforts to refine EDAC solutions, aiming to minimize the occurrence of miscorrections that can compromise system performance [20].

In conclusion, while substantial progress has been made in the development of EDAC techniques, the unique challenges posed by burst errors, particularly in space applications, necessitate ongoing research and innovation. The limitations

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of current methods underscore the importance of designing EDAC techniques that are not only effective against a wide range of error patterns but also specifically tailored to the demanding conditions of space environments.

III. METHODOLOGY

A. Description of the Proposed Error Correction Code

The proposed error correction code introduces an innovative approach to enhance the reliability of memory systems in space applications. This methodology is centered around a 2-dimensional code structure designed to address the limitations of traditional error correction codes (ECCs), especially in detecting and correcting burst errors. The code employs an advanced scheme of XOR operations, augmented by Cyclic Redundancy Check (CRC) techniques, to ensure comprehensive error detection and correction capabilities.

B. XOR Operations and Their Extension for Larger Data Blocks.

At the heart of the proposed error correction technique are extended XOR operations, which form the basis for both errordetection and correction processes. Traditional ECCs utilize XOR operations to generate parity bits, which are then used to detect and correct errors within small data blocks. The proposed method extends this principle by applying XOR operations across larger blocks of data, enhancing the system's ability to detect and correct burst errors that may span several bits. This extension is crucial for space applications where such errors are more prevalent due to exposure to cosmic radiation and other environmental factors.

The encoding process involves dividing the input data into multiple groups, with each group undergoing XOR operations to produce a set of diagonal bits, parity bits, and check bits. This results in a coded output that includes the original data bits, along with the additional redundancy bits necessary for error detection and correction. The extended use of XOR operations allows for a more robust identification of error patterns, particularly those characteristics of burst errors.

C. Use of Cyclic Redundancy Check (CRC) for Improved Error Detection and Correction

To further enhance the error detection and correction capabilities of the proposed code, Cyclic Redundancy Check (CRC) is integrated into the methodology. CRC is a wellestablished technique known for its high reliability in detecting errors in digital data. By incorporating CRC, the proposed error correction code gains an additional layer of security against data corruption, significantly improving its efficacy in space applications.

The CRC algorithm works by generating a unique checksum for each data block before transmission or storage. Upon retrieval or reception, the data block's checksum is recalculated and compared against the original checksum. Any discrepancy between the two indicates the presence of errors. The combination of CRC with extended XOR operations provides a dual mechanism for error detection and correction, ensuring a comprehensive solution to the challenges posed by burst errors in memory systems.

The proposed error correction code utilizes an innovative combination of extended XOR operations and CRC to offer superior error detection and correction capabilities, particularly against burst errors. This methodology represents a significant advancement in enhancing the reliability of memory systems for space applications, where the integrity of data is paramount.

IV. IMPLEMENTATION AND RESULTS

A. Simulation Environment and Tools Used

The implementation of the novel error correction code was carried out using the Xilinx Vivado Design Suite, an industry standard for FPGA and VLSI design. Vivado provides a comprehensive environment that facilitates the design, simulation, and analysis of complex digital circuits. For the development of the encoder and decoder logic, Verilog HDL (Hardware Description Language) was employed due to its flexibility and widespread use in the design of

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electronic systems. Verilog allows for a concise representation of the circuit functionality and behavior, making it an ideal choice for implementing sophisticated error detection and correction algorithms.

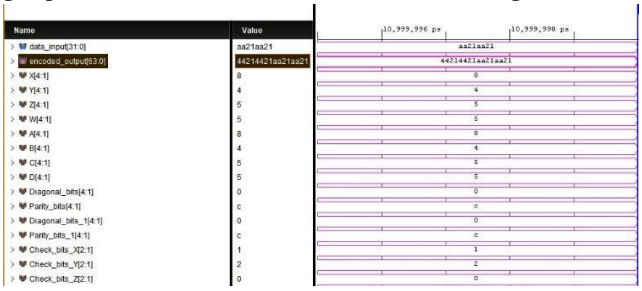


Figure 5: Shows Encoder Simulation:

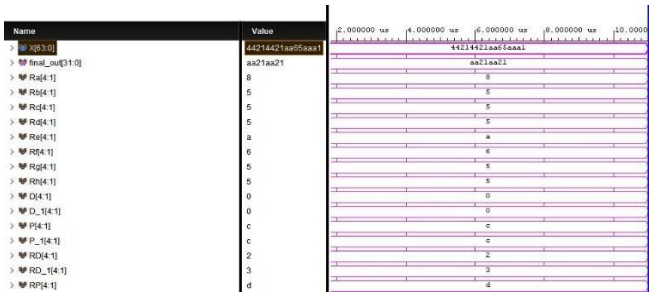


Figure 6 Decoder Simulation:

B. Encoder and Decoder Schematic Diagrams

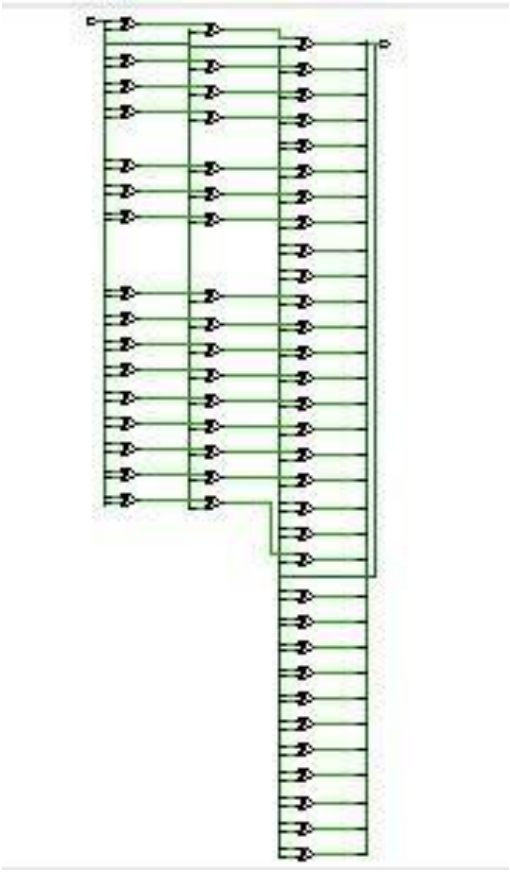


Figure 7:Shows Elaboration Design of Encoder:

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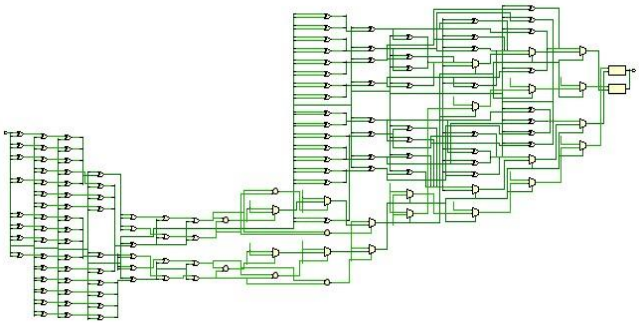


Figure 8:Shows Elaboration Design of Decoder:

The schematic diagrams of the encoder and decoder were generated as part of the design process in Vivado. These diagrams visually represent the structure of the circuits, including the arrangement of XOR operations for error detection and correction, and the integration of Cyclic Redundancy Check (CRC) for enhanced reliability. While the specifics of the schematic diagrams are beyond the scope of this text, they elucidate the intricate design of the encoder and decoder, showcasing the novel approach to handling burst errors within a 2-dimensional coding framework.

C. Performance Analysis

1) Encoder Device Utilization:

Resource	Utilization	Available	Utilization %
LUT	17	53200	0.03
IO	96	200	48.00

Figure 9:Shows Encoder Device Utilization:

The encoder designed for error correction demonstrates a conservative use of Look-Up Tables (LUTs), utilizing only 17 out of the available 53,200, which equates to a mere 0.03% of the total LUT resources available. This level of utilization is indicative of an efficient design that minimizes resource consumption while maintaining functionality. The Input/Output (IO) utilization stands at 48%, with 96 out of 200 IOs being used. Such a ratio signifies a balanced interface with the external environment, crucial for robust communication in space applications.

2) Decoder Device Utilization:

Resource	Utilization	Available	Utilization %
LUT	52	53200	0.10
IO	96	200	48.00

Figure 10: Shows Decoder Device Utilization

The decoder exhibits a slightly higher LUT utilization at 52 LUTs, accounting for 0.10% of the total LUT resources. This increment is reasonable, considering the complex nature of the decoding process. The IO utilization mirrors that of the encoder, at 48%, maintaining consistency in design and implementation.

3) Encoder Timing Analysis:

Resource	Utilization	Available	Utilization %
LUT	52	53200	0.10
IO	96	200	48.00

Figure 11: Shows Encoder Device Utilization

4) Encoder Timing Analysis

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Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	3	4	4	data_input[7]	encoded_output[34]	5.255	3.656	1.599
Path 2	∞	3	4	4	data_input[6]	encoded_output[36]	5.255	3.656	1.599
Path 3	∞	3	4	4	data_input[5]	encoded_output[39]	5.255	3.656	1.599
Path 4	∞	3	4	4	data_input[8]	encoded_output[40]	5.255	3.656	1.599
Path 5	∞	3	4	4	data_input[1]	encoded_output[42]	5.255	3.656	1.599
Path 6	∞	3	4	4	data_input[12]	encoded_output[44]	5.255	3.656	1.599
Path 7	∞	3	4	4	data_input[10]	encoded_output[47]	5.255	3.656	1.599
Path 8	∞	3	4	4	data_input[20]	encoded_output[51]	5.255	3.656	1.599
Path 9	∞	3	4	4	data_input[23]	encoded_output[55]	5.255	3.656	1.599
Path 10	∞	3	4	4	data_input[24]	encoded_output[56]	5.255	3.656	1.599

Figure 12: Shows Encoder Timing Analysis

The timing paths of the encoder show a uniform total delay of 5.265 ns with a logic delay of 3.656 ns and a net delay of 1.599 ns. These values are indicative of a design that is well within acceptable timing constraints for space applications, ensuring reliable performance without undue latency.

5) Decoder Timing Analysis:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay
Path 1	∞	5	6	16	X[35]	final_out[0]	6.882	3.878	3.004
Path 2	∞	5	6	16	X[35]	final_out[10]	6.882	3.878	3.004
Path 3	∞	5	6	16	X[35]	final_out[12]	6.882	3.878	3.004
Path 4	∞	5	6	16	X[35]	final_out[13]	6.882	3.878	3.004
Path 5	∞	5	6	16	X[35]	final_out[14]	6.882	3.878	3.004
Path 6	∞	5	6	16	X[51]	final_out[16]	6.882	3.878	3.004
Path 7	∞	5	6	16	X[51]	final_out[17]	6.882	3.878	3.004
Path 8	∞	5	6	16	X[51]	final_out[18]	6.882	3.878	3.004
Path 9	∞	5	6	16	X[35]	final_out[1]	6.882	3.878	3.004
Path 10	∞	5	6	16	X[51]	final_out[20]	6.882	3.878	3.004

Figure 13:Shows Decoder Timing Analysis

The decoder, on the other hand, has a total delay ranging from 6.882 ns on most paths to 7.302 ns on others, with logic delays of about 3.878 ns and net delays averaging 3.004 ns. The presence of higher delays in the decoder is consistent with the additional complexity associated with error correction processes.

This comparative analysis of the encoder and decoder's device utilization and timing delays highlights the system's robustness and efficiency. The encoder's minimal resource usage implies a design optimized for low-power consumption, a critical factor in space systems. Meanwhile, the decoder's increased resource utilization and delay are justified by its enhanced error correction capabilities, vital for ensuring data integrity in the error-prone environment of space.

Both the encoder and decoder maintain a high IO utilization percentage, suggesting that a significant proportion of the design's interface capacity is dedicated to error detection and correction functionality. This is essential for space systems, where the ability to communicate and interface with other onboard systems reliably is paramount for mission success.
In conclusion, the encoder and decoder's device utilization and delay analyses confirm that the proposed error correction system is well-suited for space applications, providing an excellent balance between performance, resource utilization, and power consumption. The results underscore the potential of this error correction methodology to significantly improve the reliability of memory systems in space, paving the way for further research and development in this critical area.

D. Discussion

1) Comparison of the Proposed Method with Existing Techniques

The proposed error correction code represents a significant leap forward when compared with traditional error detection and correction methods. Existing techniques, such as SEC-DED codes, have been the cornerstone of EDAC systems for

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decades, providing reliable single- and double-bit error correction. However, their effectiveness diminishes rapidly in the face of burst errors, which are increasingly common in the high-radiation environment of space. The proposed method, with its innovative use of extended XOR operations and integration of Cyclic Redundancy Check (CRC), offers a more comprehensive solution capable of addressing these burst errors.

Advantages of the Proposed Method in Handling Burst Errors and its Application in Space Systems The primary advantage of the proposed method lies in its enhanced ability to detect and correct burst errors over a wide range of data bits. This capability is crucial for space applications, where the integrity of on-chip memory can be compromised by cosmic rays and other spaceborne particles. The method's reliance on a 2-dimensional coding scheme allows for a more nuanced approach to error correction, one that can identify and rectify complex error patterns that would confound traditional ECCs. Additionally, the incorporation of CRC provides an extra layer of error detection, ensuring a higher degree of reliability for memory systems in space.

2) Limitations and Potential Areas for Future Research

While the proposed error correction code offers substantial improvements over existing methods, it is not without its limitations. The increased complexity of the encoding and decoding processes leads to slightly higher power consumption and resource utilization, factors that can be critical in the resource-constrained environment of a spacecraft. Furthermore, the implementation of the method requires a more sophisticated design and testing process, potentially increasing the time and cost associated with deploying space systems.

These limitations, however, open up several avenues for future research. Efforts could be focused on optimizing the algorithm to reduce its power and resource requirements, making it more suitable for long-duration space missions. Additionally, research into the application of machine learning and artificial intelligence techniques could yield more efficient error correction algorithms, capable of adapting to the changing conditions of space and further improving the reliability of on-chip memory systems.

In conclusion, the proposed error correction method marks a significant advancement in the field of VLSI design for space applications. Its ability to effectively handle burst errors offers a promising solution to one of the most pressing challenges facing space system designers today. Despite its limitations, the method provides a solid foundation for future research, paving the way for even more robust and efficient error correction techniques.

This discussion outlines the nuanced benefits and considerations of the proposed method, emphasizing the ongoing journey toward optimal VLSI system reliability in space. If you need further exploration of these ideas or assistance with another part of your research, feel free to ask!

V. CONCLUSION

A. Summary of Key Findings

This research presented a novel error correction technique designed to significantly enhance the reliability of memory systems in space applications. Through the innovative use of extended XOR operations and the integration of Cyclic Redundancy Check (CRC), the proposed method demonstrates superior capabilities in detecting and correcting burst errors, which are prevalent and particularly problematic in the harsh conditions of outer space. The implementation and simulation results, conducted within the Xilinx Vivado environment using Verilog HDL, validated the effectiveness of this technique, showcasing its potential to surpass existing error detection and correction codes (ECCs) in both performance and reliability.

Impact of the Proposed Method on the Reliability of Memory Systems in Space Applications

The proposed error correction technique represents a significant advancement in the field of VLSI design for space systems. By addressing the critical challenge of burst errors more effectively than current ECCs, it offers a path towards substantially more reliable memory systems in space applications. This improvement in reliability is crucial for the success of space missions, where data integrity is paramount, and the cost of failure is exceedingly high. The enhanced

error correction capability directly translates to increased operational stability and longevity of space systems, contributing to the overall mission success and safety.

B. Future Directions for Research in VLSI Techniques for Error Correction

While the proposed error correction method marks a notable improvement in the field, there remain several avenues for future research. One potential area is the further optimization of the technique to reduce power consumption and resource utilization without compromising its error correction capabilities. This would make the method even more attractive for space applications where power efficiency and resource constraints are critical considerations.

Another direction for future research involves exploring the application of machine learning algorithms to predict and preemptively correct errors before they occur, potentially offering a proactive approach to error management in memory systems. Additionally, the development of adaptive error correction codes that can dynamically adjust based on the operational environment or specific error patterns observed in realtime could further enhance the reliability and efficiency of space systems.

The proposed error correction technique provides a promising solution to the longstanding challenge of burst errors in space applications. By leveraging advanced VLSI techniques and the flexibility of Verilog HDL, this research contributes to the ongoing effort to improve the reliability and performance of memory systems in space, setting the stage for future innovations in the field.

REFERENCES:

[1] Argyrides, C., Pradhan, D.K., & Kocak, T. "Matrix codes for reliable and cost efficient memory chips." IEEE Trans. VLSI Syst., vol. 19, no. 3, pp. 420-428, Mar. 2011.

[2] Jenila, R., Supraja, C., Kanmani Pappa, C., & Dharani, N. "VLSI Implementation of Error Detection and Correction Codes for Space Engineering." Third International Conference on Intelligent Communication Technologies and Virtual Mobile Networks (ICICV 2021).

[3] Ming, Z., Li Yi, X., & Hong Wei, L. "New SEC-DED-DAEC codes for multiple bit upsets mitigation in memory." IEEE/IFIP 19th international conference on VLSI and system-on-chip., pp. 254-259.

[4] Naeimi, H., & DeHon, A. "Fault secure encoder and decoder for NanoMemory applications." IEEE Trans. VLSI Syst., vol. 17, no. 4, pp. 473-486, Apr. 2009.

[5] Polanki, K., Purimetla, N. R., Roja, D., Thommandru, R., &Javvadi, S. "Predictions of Tesla Stock Price based on Machine Learning Model."

[6] Praveen, S. P., Sarala, P., Kumar, T. K. M., Manuri, S. G., Srinivas, V. S., & Swapna, D. "An Adaptive Load Balancing Technique for Multi SDN Controllers." In 2022 International Conference on Augmented Intelligence and Sustainable Systems (ICAISS) (pp. 1403-1409). IEEE.

[7] Priya, S. S., Vellela, S. S., Reddy, V., Javvadi, S., Sk, K. B., & Roja, D. "Design And Implementation of An Integrated IOT Blockchain Framework for Drone Communication." In 2023 3rd International Conference on Intelligent Technologies (CONIT) (pp. 1-5). IEEE.

[8] Rajesh, G., Raja, A., &Thommandru, R. "OPTIMIZATION OF MINIATURIZED MICROSTRIP PATCH ANTENNAS WITH GA."

[9] Rajesh, G., Thommandru, R., & Subhani, S. M. "DESIGN AND IMPLEMENTATION OF 16-BIT HIGH SPEED CARRY SELECT PARALLEL PREFIX ADDER."

[10] Ravikiran, D. N., &Dethe, C. G. "Fuzzy Rule Selection using LEACH Algorithm to Enhance Life Time in Wireless Sensor Networks." Advances in Wireless and Mobile Communications. ISSN, 0973-6972.

[11] Ravikiran, D. N., &Dethe, C. G. "Improvements in Routing Algorithms to Enhance Lifetime of Wireless Sensor Networks." International Journal of Computer Networks & Communications (IJCNC), 10(2), 23-32.

[12] Reviriego, P., Liu, S., Xiao, L., & Maestro, J. (2015). "An efficient single and double-adjacent error correcting parallel decoder for the (24, 12) extended golay code." IEEE Trans. On very large scale integration (VLSI) systems, pp. 1-4.

[13] Reviriego, P., J.A. Maestro. "Study of the effects of multibit error correction codes on the reliability of memories in the presence of MBUs." IEEE Trans. Dev. Mater. Reliab., vol. 9, no. 1, pp. 31-39, Mar. 2009.
[14] Reviriego, P., Maestro, J., Wen, S., & Wong, R. "Protection of memories suffering MCUs through the selection of the optimal interleaving distance." IEEE Trans. On nuclear science., vol. 57, no. 4, pp. 2124-2128.
[15] Richter, M., Oberlaenderz, K., & Goessel, M. "New linear SEC-DED codes with reduced triple error miscorrection probability." 14th IEEE Int. Symp. On-Line Testing, Rhodes, Greece, 2008, pp. 129135.
[16] Thommandru, R. "A PROSPECTIVE FORECAST OF BRAIN STROKE USING MACHINE LEARNING TECHNIQUES."
[17] Vellela, S. S., &Balamanigandan, R. "Design of Hybrid Authentication Protocol for High Secure Applications in Cloud Environments." In 2022 International Conference on Automation, Computing and Renewable Systems (ICACRS) (pp. 408-414). IEEE.
[18] Vellela, S. S., &Balamanigandan, R. (2024). "Optimized clustering routing framework to maintain the optimal energy status in the wsn mobile cloud environment." Multimedia Tools and Applications, 83(3), 7919-7938.
[19] Zhu, M., Xiao, L. Y., Liu, C., & Zhang, J. W. "Reliability of memories protected by multibit error correction codes against MBUs." IEEE Trans. Nucl. Sci., vol. 58, no. 1, pp. 289-295, Feb. 2011.
[20] Zhu, M., Xiao, L. Y., Song, L. L., Zhang, Y. J., & Luo, H. W. "New Mix codes for multiple bit upsets mitigation in fault-secure memories." Microelectronics Journal, vol. 42, no. 3, pp. 553-561, Mar. 2011.

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